JEDEC STANDARD

Addendum No. 1 to JESD79-4, 3D Stacked DRAM

JESD79-4-1

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ADDENDUM No. 1 to JESD79-4, 3D STACKED SDRAM

Contents

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(From JEDEC Board Ballot JCB-16-29, formulated under the cognizance of the JC-42.3C Subcommittee on DRAM Parametrics.)

1 Scope

This document defines the 3DS DDR4 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this specification is to define the minimum set of requirements for a compliant 8 Gbit through 128 Gbit for x4, x8 3DS DDR4 SDRAM devices. This addendum was created based on the JESD79-4 DDR4 SDRAM specification. Each aspect of the changes for 3DS DDR4 SDRAM operation was considered. Any TBD's, as of the publication of this document, are under discussion by the formulating committee.

The requirement for 3DS devices compliant to this spec addendum is to have a single electrical load for the stacked devices no matter if the stack is comprised of 2, 4 or 8 devices. The I/O buffer circuitry can be built into the base SDRAM of the stack or into a separate logic buffer device. In either case (built in native circuitry or separate logic die), the assumption is that the I/O buffers are located at the bottom of the stack closest to the package substrate. All pictures and diagrams in the spec depict a master die at the bottom of the stack; it is associated with logical rank 0.

2 3DS SDRAM Package Pinout and Addressing

2.1 Overview

These ballouts have been derived from JESD79-4. The ballout comprehends x4 and x8 data widths, where x4 is a subset of the x8 ballout, and the addressing described in this section.

2.2 Pinout Description

The following table only documents differences of DDR4 3DS SDRAMs relative to the pinout description in JESD79-4.

Symbol	Type	Function
PAR	Input	Command and Address Parity Input : DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,BG0-BG1,BA0-BA1,A17-A0 and C0, C1, C2. Input parity should maintain at the rising edge of the clock and at the same time with command and address with CS_n LOW
NOTE 1 Input only pins (BG0-BG1,BA0-BA1, A0-A17, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT, C0, C1, C2 and RESET_n) do not supply termination.		

2.3 3D Stacked / DDR4 SDRAM x4 Ballout using MO-207

Ball locations in Figure 1, "3D Stacked DDR4 SDRAM x4 Ballout" show the proposed DDR4 3D Stacked SDRAM x4 ballout.

[X-ray view from package top surface]

	1	2	3	4	5	6	7	8	9	
	NC		NC				NC		NC	NC
	NC		NC				NC		NC	NC
A	VDD	VSSQ	NC				NC	VSSQ	VSS	NC
B	VPP	VDDQ	DQS_c				DQ1	VDDQ	ZQ	
C	VDDQ	DQ0	DQS_t				VDD	VSS	VDDQ	
D	VSSQ	NC	DQ2				DQ3	NC	VSSQ	
E	VSS	VDDQ	NC				NC	VDDQ	VSS	
F	VDD	C2, NC[1]	ODT				CK_t	CK_c	VDD	
G	VSS	C0	CKE				CS_n	C1, NC[2]	RFU	
H	VDD	WE_n, A14	ACT_n				CAS_n, A15	RAS_n, A16	VSS	
J	VREFCA	BG0	A10, AP				A12, BC_n	BG1	VDD	
K	VSS	BA0	A4				A3	BA1	VSS	
L	RESET_n	A6	A0				A1	A5	ALERT_n	
M	VDD	A8	A2				A9	A7	VPP	
N	VSS	A11	PAR				A17, NC[3],	A13	VDD	NC
	NC		NC				NC		NC	NC
	NC		NC				NC		NC	NC

1.This pin is not connected for 3DS devices with two or four logical ranks.
2.This pin is not connected for 3DS devices with two logical ranks.
3.This pin is not connected for 4Gb and 8Gb devices.

Figure 1 — 3D Stacked DDR4 SDRAM x4 Ballout

2.4 3D Stacked / DDR4 SDRAM x8 Ballout using MO-207

Ball locations in Figure 2, "3D Stacked DDR4 SDRAM x8 Ballout" show the proposed DDR4 3D Stacked SDRAM x8 ballout.

[X-ray view from package top surface]

	1	2	3	4	5	6	7	8	9	
	NC		NC				NC		NC	NC
	NC		NC				NC		NC	NC
A	VDD	VSSQ	TDQS_c				DBI_n, TDQS_t	VSSQ	VSS	NC
B	VPP	VDDQ	DQS_c				DQ1	VDDQ	ZQ	
C	VDDQ	DQ0	DQS_t				VDD	VSS	VDDQ	
D	VSSQ	DQ4	DQ2				DQ3	DQ5	VSSQ	
E	VSS	VDDQ	DQ6				DQ7	VDDQ	VSS	
F	VDD	C2, NC[1]	ODT				CK_t	CK_c	VDD	
G	VSS	C0	CKE				CS_n	C1, NC[2]	RFU	
H	VDD	WE_n, A14	ACT_n				CAS_n, A15	RAS_n, A16	VSS	
J	VREFCA	BG0	A10, AP				A12, BC_n	BG1	VDD	
K	VSS	BA0	A4				A3	BA1	VSS	
L	RESET_n	A6	A0				A1	A5	ALERT_n	
M	VDD	A8	A2				A9	A7	VPP	
N	VSS	A11	PAR				NC	A13	VDD	NC
	NC		NC				NC		NC	NC
	NC		NC				NC		NC	NC

1.This pin is not connected for 3DS devices with two or four logical ranks.
2.This pin is not connected for 3DS devices with two logical ranks.

Figure 2 — 3D Stacked DDR4 SDRAM x8 Ballout

2.5 Logical Rank Addressing

The 3DS package is organized into two, four or eight logical ranks.

For DDR4 3DS devices, the logical ranks are selected by the Chip ID bus C[2:0].

The functional behavior of logical rank(s) should not deviate from monolithic DDR4 SDRAMs (specified in JESD79-4A), except when noted in this document. Each logical rank may be implemented as a single slice but the DDR4 3DS addendum doesn't require this to be the case.

2.6 3D Stack Organizations

Table 1, "Supported 3D Stack Organizations," indicates valid configurations supported by the DDR4 3DS addendum.

Table 1 — Supported 3D Stack Organizations

Logical Ranks	# of CS_n	Chip ID	# of CKE	# of ODT
2	1	C0	1	1
4	1	C0, C1	1	1
8	1	C0, C1, C2	1	1

Figure 3, Figure 4, and Figure 5 show one architectural diagram per row of Table 1. For the names of the these figures the standard *3DS configuration notation* LR-CS-CKE-ODT is used where LR indicates the number of logical ranks, CS_n indicates the number of chip select inputs, CKE indicates the number of CKE inputs and ODT indicates the number of ODT inputs. Since there is only one valid configuration for each number of logical ranks, this document will typical use the abbreviations 2H, 4H and 8H to describe 3DS devices with two, four or eight logical ranks.

2.7 3DS SDRAM System Addressing

3DS addressing scheme for DDR4 3DS devices is explained in section 2.8. This document comprehends using these 3DS devices in RDIMM and LRDIMM applications with x4 or x8 3DS SDRAMs.

2.8 DDR4 3DS Stack Addressing Table

Table 2, Table 3 and Table 4 indicate the address and select pins that are used for different configurations of 3DS stacks.

The DDR4 3DS devices may be derived from monolithic DDR4 devices. Therefore the address signals used within a logical rank are identical to the address signals used by a monolithic DRAM of the same density. Logical Rank 0 is considered to be associated with the master die.

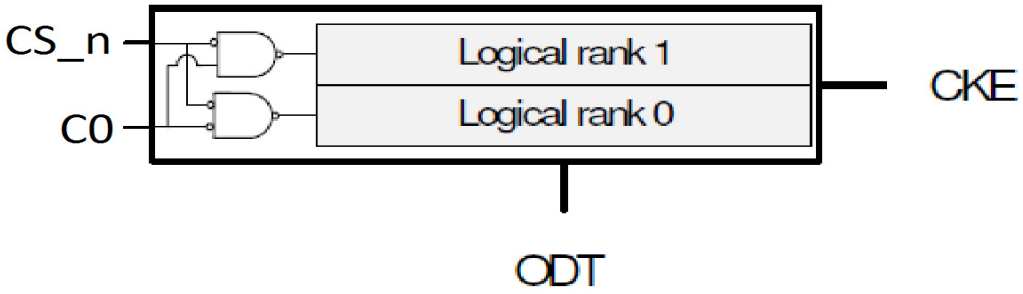


Figure 3 — 2-1-1-1 Device (2H)

Table 2 — DDR4 Address Table: 2H Stacked SDRAM

DDR4 3DS Address Table: 2H 3D Stacked SDRAM									
3DS Logical Rank Organization						3DS Package Organization			
Density	x4 Page Size	x8 Page Size	MSB Address			Capacity	Logical Rank	CS_n	C0
			Col	Row					
				x4 Die	x8 Die				
4 Gb	512 B	1 KB	A9	A15	A14	8 Gb	0	L	L
							1	L	H
8 Gb	512 B	1 KB	A9	A16	A15	16 Gb	0	L	L
							1	L	H
16 Gb	512 B	1 KB	A9	A17	A16	32 Gb	0	L	L
							1	L	H

2.8 DDR4 3DS Stack Addressing Table (cont'd)

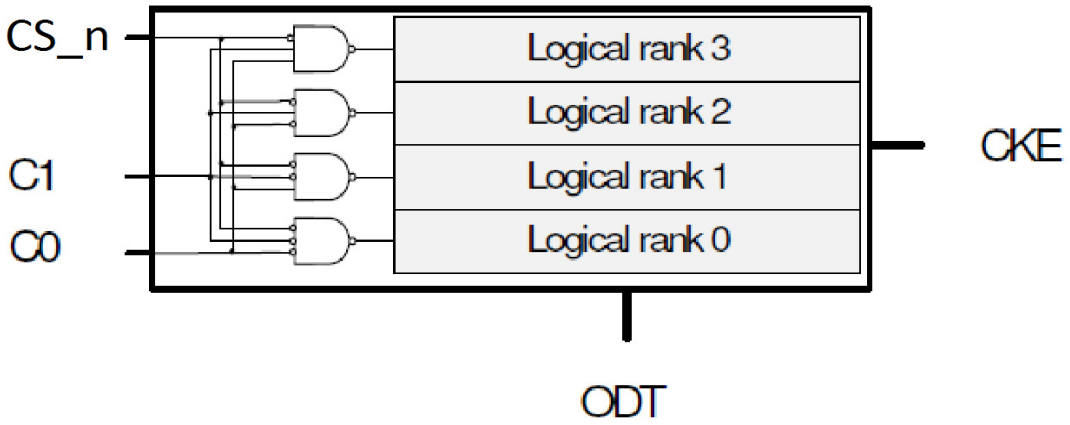


Figure 4 — 4-1-1-1 Device (4H)

Table 3 — DDR4 Address Table: 4H Stacked SDRAM

DDR4 3DS Address Table: 4H 3D Stacked SDRAM										
3DS Logical Rank Organization						3DS Package Organization				
Density	x4 Page Size	x8 Page Size	MSB Address			Capacity	Logical Rank	CS_n	C1	C0
			Col	Row						
				x4 Die	x8 Die					
4 Gb	512 B	1 KB	A9	A15	A14	16 Gb	0	L	L	L
							1	L	L	H
							2	L	H	L
							3	L	H	H
8 Gb	512 B	1 KB	A9	A16	A15	32 Gb	0	L	L	L
							1	L	L	H
							2	L	H	L
							3	L	H	H
16 Gb	512 B	1 KB	A9	A17	A16	64 Gb	0	L	L	L
							1	L	L	H
							2	L	H	L
							3	L	H	H

2.8 DDR4 3DS Stack Addressing Table (cont'd)

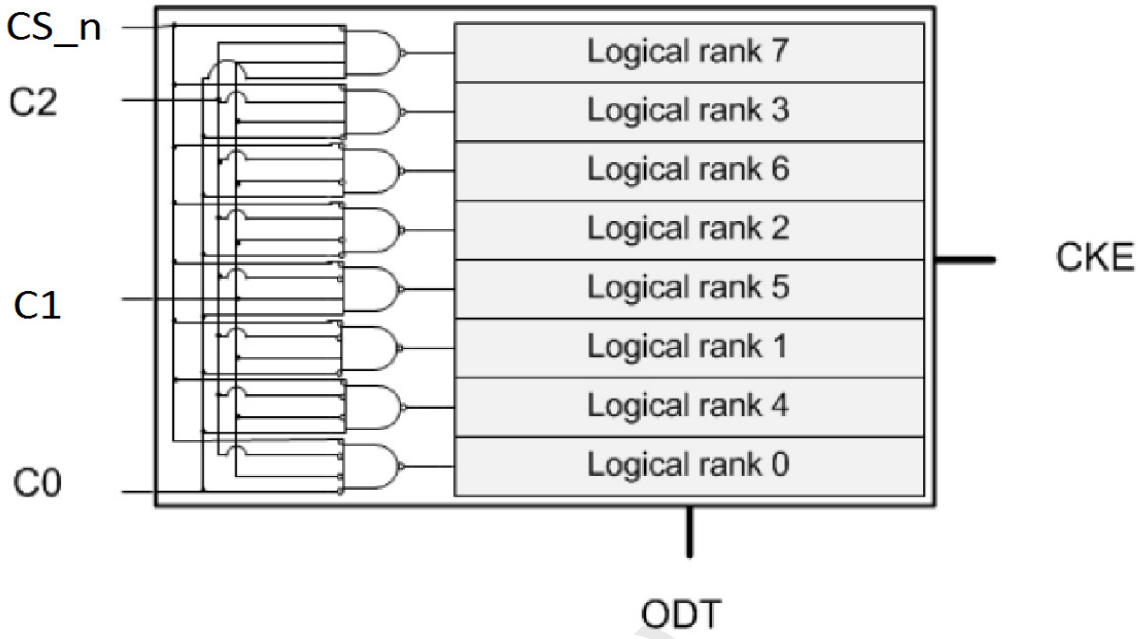


Figure 5 — 8-1-1-1 Device (8H)

2.8 DDR4 3DS Stack Addressing Table (cont'd)

Table 4 — DDR4 Address Table: 8H Stacked SDRAM

DDR4 3DS Address Table: 8H 3D Stacked SDRAM											
3DS Logical Rank Organization						3DS Package Organization					
Density	x4 Page Size	x8 Page Size	MSB Address			Capacity	Logical Rank	CS_n	C2	C1	C0
			Col	Row							
				x4 Die	x8 Die						
4 Gb	512 B	1 KB	A9	A15	A14	32 Gb	0	L	L	L	L
							1	L	L	L	H
							2	L	L	H	L
							3	L	L	H	H
							4	L	H	L	L
							5	L	H	L	H
							6	L	H	H	L
							7	L	H	H	H
8 Gb	512 B	1 KB	A9	A16	A15	64 Gb	0	L	L	L	L
							1	L	L	L	H
							2	L	L	H	L
							3	L	L	H	H
							4	L	H	L	L
							5	L	H	L	H
							6	L	H	H	L
							7	L	H	H	H
16 Gb	512 B	1 KB	A9	A17	A16	128 Gb	0	L	L	L	L
							1	L	L	L	H
							2	L	L	H	L
							3	L	L	H	H
							4	L	H	L	L
							5	L	H	L	H
							6	L	H	H	L
							7	L	H	H	H

NOTE These diagrams show only the logical organizations of these devices. No 1:1 relationship to physical organizations is implied. The Logical Rank 0 is considered the "master die", regardless of its physical arrangement.

2.9 Logical Rank, Bank Group and Bank Selection

DDR4 3DS devices can accommodate up to 128 banks, organized into 32 independent bank groups of 4 dependent banks each. The 128 banks are distributed among 8 logical ranks, each of which has 16 banks, organized into 4 independent bank groups of 4 dependent banks each. Table 5 shows how the logical ranks and bank groups in a DDR4 3DS device are selected. Table 6 shows how the individual banks are selected.

Table 5 — Logical rank and Bank Group Selection

					C2	C1	C0	CS_n
Logical Rank 7	31	30	29	28	1	1	1	0
Logical Rank 6	27	26	25	24	1	1	0	0
Logical Rank 5	23	22	21	20	1	0	1	0
Logical Rank 4	19	18	17	16	1	0	0	0
Logical Rank 3	15	14	13	12	0	1	1	0
Logical Rank 2	11	10	9	8	0	1	0	0
Logical Rank 1	7	6	5	4	0	0	1	0
Logical Rank 0	3	2	1	0	0	0	0	0
	Address by BG[1:0] =							
	11	10	01	00				

Table 6 — Bank Selection

Logical Rank 7	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112
Logical Rank 6	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
Logical Rank 5	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
Logical Rank 4	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
Logical Rank 3	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
Logical Rank 2	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Logical Rank 1	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Logical Rank 0	15	14	13	12	11	10	9	8	7	6	5	4	Bank Group 0			

Addressed by BA[1:0] =

11	10	01	00

Addressed by BG[1:0] =

11	10	01	00

3 Functional Description

3.1 Simplified State Diagram

There is no difference between the simplified state diagrams for DDR4 and 3DS DDR4. Situations involving more than one bank, and multiple logical ranks are not reflected in the simple state diagram for DDR4 and are not captured in full detail.

3.2 Basic Functionality

The 3DS DDR4 SDRAM is a 2H, 4H or 8H stacked high-speed dynamic random-access memory with each logical rank configured as a 16-bank SDRAM (organized into four bank groups of four banks each). The 3DS SDRAM has 32, 64 or 128 physical banks available internally, depending on the number of logical ranks. The 3DS DDR4 SDRAM retains the use of an 8n pre-fetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the 3DS DDR4 SDRAM consists of a single 8n-bit wide, one clock data transfer at the internal SDRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

3.3 Reset Signal and Initialization Procedure

Prior to normal operation, the 3DS DDR4 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions and device operation.

A single reset pin with a single load is available per 3DS device. It is expected that the entire stack of SDRAMs within the package reset as per DDR4 specification. After RESET_n is de-asserted, the SDRAM will start internal state initialization; this will be done independently of external clocks. All steps in the DDR4 initialization sequence must be followed. No additional steps are required for 3DS DDR4 devices but the unique nature of 3DS devices (which have a single external I/O structure shared by all logical ranks of the entire device) has to be considered when programing the SDRAM mode register bits (see next section for details).

3.4 Mode Register Definition

For application flexibility, various functions, features and modes are programmable in seven Mode Registers. One set of registers controls the entire stack regardless if the 3DS stack has two, four or eight logical ranks, and they must be programmed via a Mode Register Set (MRS) command.

For 3DS DDR4 stacks configured as n logical ranks, a single set of MRS registers is addressed by the Chip Select signal (CS_n) as shown in Table 7.

3.4 Mode Register Definition (cont'd)

Table 7 — Simplified Truth Table for MRS Command

DRAM Command	CS_n	C2	C1	C0	Logical Rank0	Logical Rank1	Logical Rank2	Logical Rank3	Logical Rank4	Logical Rank5	Logical Rank6	Logical Rank7	Notes
Mode Register Set	L	V	V	V	MRS	MRS	MRS	MRS	MRS	MRS	MRS	MRS	1
Mode Register Set	H	V	V	V	DES	DES	DES	DES	DES	DES	DES	DES	1
Any other command	H	V	V	V	DES	DES	DES	DES	DES	DES	DES	DES	1

NOTE 1 "V" means H or L (but a defined logic level).

Programming the register fields for a stacked device has some special considerations. Waiting for tMRD is required between two MRS commands issued to a 3DS SDRAM. After an MRS command is given, waiting for tMOD is required before a non-MRS command can be issued to any of the logical ranks in the stack.

Due to the difference between CAS Latency and nRCD, DDR4 3DS devices require a different Additive Latency definition than mono DDR4 SDRAMs. The changes to MR1 are shown in Table 10.

Table 8 — MR0 Definition for DDR4 3DS

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A11:A9	WR and RTP	Write Recovery and Read to Precharge for auto precharge see respective table in JESD79-4)
A8	DLL Reset	0 = NO 1 = Yes
A7	TM	0 = Normal 1 = Test
A12, A6:A4, A2	CAS Latency[2]	(see Table 9)
A3	Read Burst Type	0 = Sequential 1 = Interleave
A1:A0	Burst Length	00 = 8 (Fixed) 01 = BC4 or 8 (on the fly) 10 = BC4 (Fixed) 11 = Reserved

NOTE 1 Reserved for Register control word setting. DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

NOTE 2 The table only shows the encodings for a given Cas Latency. For actual supported Cas Latency, please refer to speedbin tables for each frequency which device supports. A12 is an additional bit to encode for Cas Latency. Hence availability of A12=1 could depend on Device.

3.4 Mode Register Definition (cont'd)

Table 9 — CAS Latency

A12	A6	A5	A4	A2	CAS Latency
0	0	0	0	0	9
0	0	0	0	1	10
0	0	0	1	0	11
0	0	0	1	1	12
0	0	1	0	0	13
0	0	1	0	1	14
0	0	1	1	0	15
0	0	1	1	1	16
0	1	0	0	0	18
0	1	0	0	1	20
0	1	0	1	0	22
0	1	0	1	1	24
0	1	1	0	0	23
0	1	1	0	1	17
0	1	1	1	0	19
0	1	1	1	1	21
1	0	0	0	0	25
1	0	0	0	1	26
1	0	0	1	0	27
1	0	0	1	1	28
1	0	1	0	0	Reserved for 29
1	0	1	0	1	30
1	0	1	1	0	Reserved for 31
1	0	1	1	1	32
1	1	0	0	0	Reserved

3.4 Mode Register Definition (cont'd)

Table 10 — MR1 Definition for DDR4 3DS

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[3]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Qoff[1]	0 = Output buffer enabled 1 = Output buffer disabled
A11	TDQS enable	0 = Disable 1 = Enable
A10, A9, A8	RTT_NOM	(see respective table in JESD79-4)
A7	Write Leveling Enable	0 = Disable 1 = Enable
A6, A5	RFU	0 = must be programmed to 0 during MRS
A4, A3	Additive Latency[4]	00 = 0(AL disabled) 10 = CL-2 01 = Reserved 11 = CL-3
A2, A1	Output Driver Impedance Control	(see respective table in JESD79-4)
A0	DLL Enable	0 = Disable[2] 1 = Enable

NOTE 1 Outputs disabled - DQs, DQS_ts, DQS_cs.

NOTE 2 States reversed to "0 as Disable" with respect to DDR3.

NOTE 3 Reserved for Register control word setting. DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

NOTE 4 When the gap between tAA and tRCD is bigger than 2 clock cycles, host should increment tRCD accordingly to use AL, knowing that DDR4 3DS only supports AL of CL-2 and CL-3.

3.4 Mode Register Definition (cont'd)

Table 11 — MR2 Definition for DDR4 3DS

Address	Operating Mode	Description	
C2 , C1 , C0	TRR Mode Chip ID	000 = LR0 100 = LR4 001 = LR1 101 = LR5 010 = LR2 110 = LR6 011 = LR3 111 = LR7	DDR4 3DS only
BG1	RFU	0 = must be programmed to 0 during MRS	No change from JESD79-4
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[1]	
A17	RFU	0 = must be programmed to 0 during MRS	
A13	RFU	0 = must be programmed to 0 during MRS	
A12	Write CRC	0 = Disable 1 = Enable	
A11	RFU	0 = must be programmed to 0 during MRS	
A10:A9	RTT_WR	(see respective table in JESD79-4)	
A8	RFU	0 = must be programmed to 0 during MRS	
A7:A6	Low Power Array Self Refresh (LP ASR)	00 = Manual Mode (Normal Operaing Temperature Range) 01 = Manual Mode (Reduced Operating Temperature Range) 10 = Manual Mode (Extended Operating Temperature Range) 11 = ASR Mode (Auto Self Refresh)	
A5:A3	CAS Write Latency(CWL)	(see respective table in JESD79-4)	
A2:A0	RFU	0 = must be programmed to 0 during MRS	

NOTE 1 Reserved for Register control word setting.DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

4 SDRAM Command Description and Operation

4.1 ACTIVATE Command

In a 3D Stacked DDR4 SDRAM the single chip select pin and the C[2:0] pins select the logical rank - see Table 12.

The value on the BA0 - BA1 and BG0 - BG1 inputs selects the bank, the chip ID inputs select the logical ranks and the address provided on inputs A0-A17 selects the row. This row remains open (or active) for accesses until a precharge command is issued to that bank in that logical rank. A PRECHARGE command must be issued (to that bank in that logical rank) before opening a different row in the same bank in the same logical rank.

The minimum time interval between successive ACTIVATE commands to the same bank of a DDR SDRAM is defined by tRC. The minimum time interval between successive ACTIVATE commands to different banks within the same bank group of a DDR4 SDRAM is defined by tRRD_L (Min). The minimum time interval between successive ACTIVATE commands to different banks within different bank groups of a DDR4 SDRAM is defined by tRRD_S (Min). For a DDR4 3DS device, the timing parameters that applies to successive ACTIVATE commands to different banks in the same logical rank are defined as tRRD_S_slr (Min) and tRRD_L_slr (Min). The timing parameter that applies to successive ACTIVATE commands to different logical ranks is defined as tRRD_dlr (Min).

No more than four bank ACTIVATE commands may be issued in a given tFAW_slr (Min) period to the same logical rank. For all logical ranks in a 3DS device, the tFAW_dlr timing constraint applies, i.e., no more than four bank ACTIVATE commands to the whole 3DS SDRAM may be issued in a given tFAW_dlr (Min) period.

The timing restrictions covering ACTIVATE commands are documented in Table 43.

Table 12 — Truth Table for ACTIVATE Command

Symbol	CS_n	C2	C1	C0	Logical Rank0	Logical Rank1	Logical Rank2	Logical Rank3	Logical Rank4	Logical Rank5	Logical Rank6	Logical Rank7
ACTIVATE (ACT)	L	L	L	L	**ACT**	DES	DES	DES	DES	DES	DES	DES
ACTIVATE (ACT)	L	L	L	H	DES	**ACT**	DES	DES	DES	DES	DES	DES
ACTIVATE (ACT)	L	L	H	L	DES	DES	**ACT**	DES	DES	DES	DES	DES
ACTIVATE (ACT)	L	L	H	H	DES	DES	DES	**ACT**	DES	DES	DES	DES
ACTIVATE (ACT)	L	H	L	L	DES	DES	DES	DES	**ACT**	DES	DES	DES
ACTIVATE (ACT)	L	H	L	H	DES	DES	DES	DES	DES	**ACT**	DES	DES
ACTIVATE (ACT)	L	H	H	L	DES	DES	DES	DES	DES	DES	**ACT**	DES
ACTIVATE (ACT)	L	H	H	H	DES	DES	DES	DES	DES	DES	DES	**ACT**
Any command	H	V	V	V	DES	DES	DES	DES	DES	DES	DES	DES

NOTE "V" means H or L (but a defined logic level).

4.2 Precharge and Precharge All Commands

The Single Bank Precharge (PRE) and Precharge All Banks (PREA) commands apply only to a single logical rank of a 3D Stacked SDRAM. PRE commands (or PRE commands to each open bank) have to be issued to all logical ranks with open banks before the device can enter Self Refresh mode.

DDR4 3D Stacked SDRAMs have the same values for tRP, tRTP, tRAS and tDAL as planar DDR4 SDRAMs of the same frequency.

Table 13 and Table 14 show the truth tables for Precharge and Precharge All commands.

Table 13 — Truth Table for Precharge

DRAM Command	CS_n	C2	C1	C0	Logical Rank0	Logical Rank1	Logical Rank2	Logical Rank3	Logical Rank4	Logical Rank5	Logical Rank6	Logical Rank7	Notes
Precharge (PRE)	L	L	L	L	**PRE**	DES	DES	DES	DES	DES	DES	DES	1, 3
Precharge (PRE)	L	L	L	H	DES	**PRE**	DES	DES	DES	DES	DES	DES	1, 3
Precharge (PRE)	L	L	H	L	DES	DES	**PRE**	DES	DES	DES	DES	DES	1, 3
Precharge (PRE)	L	L	H	H	DES	DES	DES	**PRE**	DES	DES	DES	DES	1, 3
Precharge (PRE)	L	H	L	L	DES	DES	DES	DES	**PRE**	DES	DES	DES	1, 3
Precharge (PRE)	L	H	L	H	DES	DES	DES	DES	DES	**PRE**	DES	DES	1, 3
Precharge (PRE)	L	H	H	L	DES	DES	DES	DES	DES	DES	**PRE**	DES	1, 3
Precharge (PRE)	L	H	H	H	DES	DES	DES	DES	DES	DES	DES	**PRE**	1, 3
Any command	H	V	V	V	DES	DES	DES	DES	DES	DES	DES	DES	2

NOTE 1 Precharge only to the same selected bank within selected logical rank(s)
NOTE 2 "V" means H or L (but a defined logic level)
NOTE 3 A10=L

Table 14 — Truth Table for Precharge All

DRAM Command	CS_n	C2	C1	C0	Logical Rank0	Logical Rank1	Logical Rank2	Logical Rank3	Logical Rank4	Logical Rank5	Logical Rank6	Logical Rank7	Notes
Precharge All (PREA)	L	L	L	L	**PREA**	DES	DES	DES	DES	DES	DES	DES	1, 3
Precharge All (PREA)	L	L	L	H	DES	**PREA**	DES	DES	DES	DES	DES	DES	1, 3
Precharge All (PREA)	L	L	H	L	DES	DES	**PREA**	DES	DES	DES	DES	DES	1, 3
Precharge All (PREA)	L	L	H	H	DES	DES	DES	**PREA**	DES	DES	DES	DES	1, 3
Precharge All (PREA)	L	H	L	L	DES	DES	DES	DES	**PREA**	DES	DES	DES	1, 3
Precharge All (PREA)	L	H	L	H	DES	DES	DES	DES	DES	**PREA**	DES	DES	1, 3
Precharge All (PREA)	L	H	H	L	DES	DES	DES	DES	DES	DES	**PREA**	DES	1, 3
Precharge All (PREA)	L	H	H	H	DES	DES	DES	DES	DES	DES	DES	**PREA**	1, 3
Any command	H	V	V	V	DES	DES	DES	DES	DES	DES	DES	DES	2

NOTE 1 Precharge all banks only in selected logical rank(s)
NOTE 2 "V" means H or L (but a defined logic level)
NOTE 3 A10=H

4.3 Read and Write Commands

In a DDR4 3D Stacked SDRAM the single select pin and the C[2:0] pins select the logical rank.

The DDR4 3DS command to command timings are shown in Table 15 and Table 16.

Table 15 — Minimum Read and Write Command Timings for 2H and 4H devices

Logical Rank	Bank Group	Timing Parameter	DDR4 1600 3DS	DDR4 1866 3DS	DDR4 2133 3DS	DDR4 2400 3DS	DDR4 2666 3DS	DDR4 3200 3DS	Units	Note
same	same	Minimum Read to Read	5	5	6	6	TBD	TBD	nCK	1
		Minimum Write to Write								
		Minimum Read to Write	CL - CWL + RBL / 2 + 1 tCK + tWPRE							1, 2
		Minimum Read after Write	CWL + WBL / 2 + tWTR_L							1, 3
	different	Minimum Read to Read	4	4	4	4	4	TBD	nCK	1
		Minimum Write to Write								
		Minimum Read to Write	CL - CWL + RBL / 2 + 1 tCK + tWPRE							1, 2
		Minimum Read after Write	CWL + WBL / 2 + tWTR_S							1, 3
different	same or different	Minimum Read to Read	4	4	5 (4) (optional)	5	TBD	TBD	nCK	1
		Minimum Write to Write								
		Minimum Read to Write	CL - CWL + RBL / 2 + 1 tCK + tWPRE							1, 2
		Minimum Read after Write	CWL + WBL / 2 + tWTR_S							1, 3

NOTE 1 These timings require extended calibrations times tZQinit and tZQCS (values TBD).

NOTE 2 RBL: Read burst length associated with Read command.
RBL = 8 for fixed 8 and on-the-fly mode 8.
RBL = 4 for fixed BC4 and on-the-fly mode BC4.

NOTE 3 WBL: Write burst length associated with Write command.
WBL = 8 for fixed 8 and on-the-fly mode 8 or BC4.
WBL = 4 for fixed BC4 only.

4.3 Read and Write Commands (cont'd)

Table 16 — Minimum Read and Write Command Timings for 8H devices

Logical Rank	Bank Group	Timing Parameter	DDR4 1600 3DS	DDR4 1866 3DS	DDR4 2133 3DS	DDR4 2400 3DS	DDR4 2666 3DS	DDR4 3200 3DS	Units	Note
same	same	Minimum Read to Read	TBD	TBD	TBD	TBD	TBD	TBD	n_{CK}	1
		Minimum Write to Write								
		Minimum Read to Write	TBD							1
		Minimum Read after Write	TBD							1
	different	Minimum Read to Read	TBD	TBD	TBD	TBD	TBD	TBD	n_{CK}	1
		Minimum Write to Write								
		Minimum Read to Write	TBD							1
		Minimum Read after Write	TBD							1
different	same or different	Minimum Read to Read	TBD	TBD	TBD	TBD	TBD	TBD	n_{CK}	1
		Minimum Write to Write								
		Minimum Read to Write	TBD							1
		Minimum Read after Write	TBD							1

NOTE 1 These timings require extended calibrations times tZQinit and tZQCS (values TBD).

4.4 Refresh Command

No more than one logical rank Refresh Command can be initiated simultaneously to DDR4 3D Stacked SDRAMs as shown in Table .

The minimum refresh cycle time to a single logical rank (=tRFC_slr) has the same value as tRFC for a planar DDR4 SDRAM of the same density as the logical rank.

The minimum time between issuing refresh commands to different logical ranks is specified as tRFC_dlr. After a Refresh command to a logical rank, other valid commands can be issued before tRFC_dlr to the other logical ranks that are not the target of the refresh.

Table 17 — Truth Table for Refresh Command

DRAM Command	CS_n	C2	C1	C0	Logical Rank0	Logical Rank1	Logical Rank2	Logical Rank3	Logical Rank4	Logical Rank5	Logical Rank6	Logical Rank7	Notes
Refresh (REF)	L	L	L	L	**REF**	DES	DES	DES	DES	DES	DES	DES	1
Refresh (REF)	L	L	L	H	DES	**REF**	DES	DES	DES	DES	DES	DES	1
Refresh (REF)	L	L	H	L	DES	DES	**REF**	DES	DES	DES	DES	DES	1
Refresh (REF)	L	L	H	H	DES	DES	DES	**REF**	DES	DES	DES	DES	1
Refresh (REF)	L	H	L	L	DES	DES	DES	DES	**REF**	DES	DES	DES	1
Refresh (REF)	L	H	L	H	DES	DES	DES	DES	DES	**REF**	DES	DES	1
Refresh (REF)	L	H	H	L	DES	DES	DES	DES	DES	DES	**REF**	DES	1
Refresh (REF)	L	H	H	H	DES	DES	DES	DES	DES	DES	DES	**REF**	1
Any command	H	V	V	V	DES	DES	DES	DES	DES	DES	DES	DES	1, 2

NOTE 1 CKE=H.
NOTE 2 "V" means H or L (but a defined logic level).

In general, a Refresh command needs to be issued to each logical rank in 3D Stacked DDR4 SDRAM regularly every tREFI_slr interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 Refresh commands per logical rank can be postponed during operation of the 3D stacked DDR4 SDRAM, meaning that at no point in time more than a total of 8 Refresh commands are allowed to be postponed per logical rank. In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to 9 × tREFI_slr. A maximum of 8 additional Refresh commands can be issued in advance (“pulled in”) per logical rank, with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8 Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to 9 × tREFI_slr. At any given time, a maximum of 16 REF commands per logical rank can be issued within 2 x tREFI_slr. Self-Refresh Mode may be entered with a maximum of eight Refresh commands per logical rank being postponed. After exiting Self-Refresh Mode with one or more Refresh commands postponed, additional Refresh commands may be postponed to the extent that the total number of postponed Refresh commands (before and after the Self-Refresh) will never exceed eight per logical rank. During Self-Refresh Mode, the number of postponed or pulled-in REF commands does not change.

4.5 Self-Refresh Operation and Power-Down Modes

The CKE functionality should adhere to the DDR4 specification for planar DDR4 SDRAMs. Since there is only one CKE pin per 3DS device, all logical ranks enter self refresh and power down together, as shown in Table 18.

Table 18 — Truth Table for SRE and PD

DRAM Command	CS_n	C2	C1	C0	Logical Rank0	Logical Rank1	Logical Rank2	Logical Rank3	Logical Rank4	Logical Rank5	Logical Rank6	Logical Rank7	Notes
Refresh (REF)	L	V	V	V	SRE	SRE	SRE	SRE	SRE	SRE	SRE	SRE	1, 2
Refresh (REF)	H	V	V	V	PDE	PDE	PDE	PDE	PDE	PDE	PDE	PDE	1, 2
NOP	L	V	V	V	PDE	PDE	PDE	PDE	PDE	PDE	PDE	PDE	1, 2
Any command	H	V	V	V	PDE	PDE	PDE	PDE	PDE	PDE	PDE	PDE	1, 2

NOTE 1 "V" means H or L (but a defined logic level).
NOTE 2 With CKE H-->L.

Self-Refresh exit (SRX) and power-down exit (PDX) apply to all logical ranks in a 3D Stacked device and is caused by the Low-to-High transition of the single CKE pin.

A Deselect command must be used for SRX.

A Deselect command must be used for PDX.

3D Stacked SDRAMs have the same values of all parameters for Self Refresh Timings and Power Down Timings as planar DDR4 SDRAMs of the same frequency. Specification of tXS DDR4 3DS has been modified with Refresh Parameter by Logical Rank Density.

Once a Self-Refresh Exit command (SRX, combination of CKE going high and either NOP or Deselect on command bus) is registered, a delay of at least tXS must be satisfied before a valid command not requiring a locked DLL can be issued to the device to allow for any internal refresh in progress.The use of Self-Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self-Refresh mode. Upon exit from Self-Refresh, the DDR4 3D stacked SDRAM requires a minimum of one extra refresh command to all logical Ranks (each refresh period of tRFC_slr), before it is put back into Self-Refresh Mode.

4.6 Write Leveling

The memory controller initiates Leveling mode of all SDRAMs by setting bit A7 of MR1 to 1. Upon entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only DESELECT commands are allowed, as well as an MRS command to exit write leveling mode. Since the controller levels one rank at a time, the output of other physical ranks must be disabled by setting MR1 bit A12 to 1.

4.7 ZQ Calibration Commands

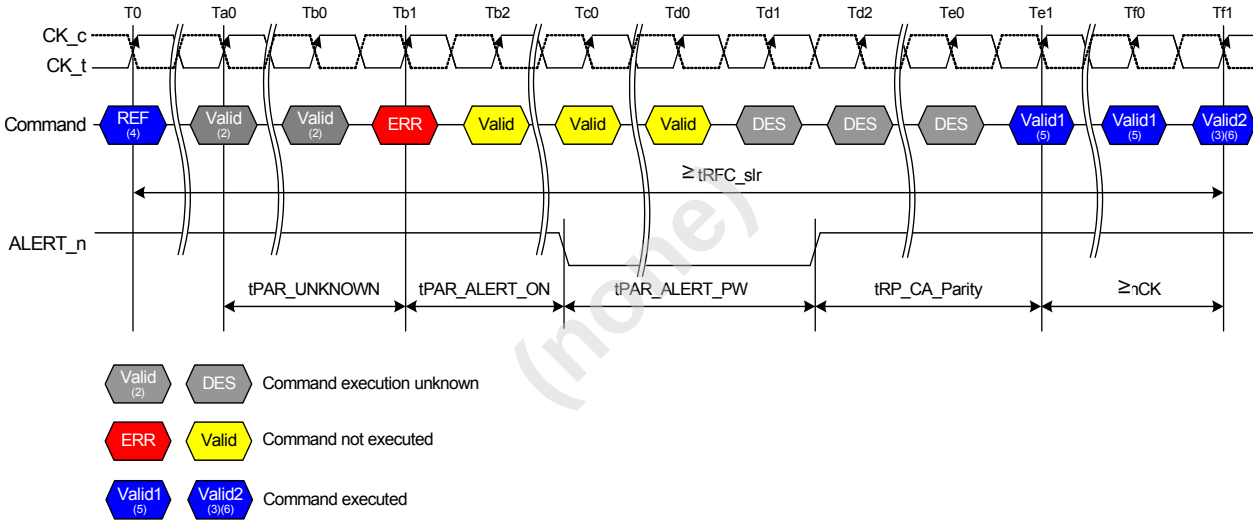
Each 3DS package will have a single ZQ calibration pin, independent of the number of logical ranks in the stack. Since there is only one I/O per device, the ZQ pin should be associated with the master die.

The calibration procedure and the result should adhere to JEDEC DDR4 component specification (JESD79-4). The host may issue ZQ calibration command to each logical rank. If a ZQ command is issued to the master logical rank ZQ calibration will be performed. If a ZQ command is issued to a non-master rank the ZQ command may be ignored, however ZQ calibration timings must be observed. The SDRAM can choose to ignore the ZQ commands to the non-master logical rank or execute the calibration of the I/O attached to the master die.

4.8 Command Address Parity (CA Parity)

C/A Parity signal (PAR) covers ACT_n, RAS_n, CAS_n, WE_n and the address bus including bank address, bank group bits and chip ID bits C[2:0]. The control signals CKE, ODT and CS_n are not included. (e.g., for a 4 Gbit x4 monolithic device, parity is computed across BG0, BG1, BA1, BA0, A16/ RAS_n, A15/CAS_n, A14/WE_n, A13-A0 and ACT_n). (DRAM should internally treat any unused address pins as 0's, e.g., if a common die has stacked pins C[2:0] but the device is used in a monolithic or less than 8H stacked application then the unused address pins should internally be treated as 0's).

When Refresh commands are issued to logical ranks prior to a Error command on the other rank, 3DS DDR4 shall finish the on-going Refresh operation. Upon Alert Pulse Width deactivation, DRAM conducts Precharge-All operation to the logical ranks which are not on Refresh operation to make them ready for valid commands. After tRP_CA_Parity from the end of tPAR_ALERT_PW, valid commands can be issued to the logical ranks which do not have on-going Refresh operation. Valid commands, including MRS, to the logical ranks with on-going Refresh can be issued after both tRFC_slr and tRP_CA_Parity are met as illustrated in Figure 6.



NOTE 1 DRAM is emptying queues, Precharge All and parity cheching off until Parity Error Status bit cleared.
NOTE 2 Command execution is unkown the corresponding DRAM internal state change may or may not occur. The DRAM controller should consider both cases and make sure that the command sequence meets the specifications.
NOTE 3 Normal operation with parity latency (CA Parity Persistent Error Mode Disabled). Parity checking off until Parity Error Status bit cleared.
NOTE 4 When REF is issued in tPAR_UNKNOWN range, REF may not be executed. But, host must wait tRFC_slr to issue valid commands to the same logical rank.
NOTE 5 Valid commands to the rank with no on-going REFare available.
NOTE 6 Valid commands, including MRS, to the rank with on-going REF are available.

Figure 6 — DDR4 3DS SDRAM Refresh Operation

Table 19 — Timing delay for Valid commands from Alert Pulse deassertion

Parameter	Symbol	DDR4-1600, 1866, 2133, 2400	DDR4-2666, 3200	Units	Note
Minimum time for valid commnads except for MRS to the logical ranks that do not conduct REF	tRP_CA_Parity	TBD	TBD	n_{CK}	

4.9 Target Row Refresh (TRR)

For DRAM to operate TRR function independantly on the selected logical rank, logical rank information (C0, C1 and C2) should be given to DRAM at the TRR mode entry (MR2 A13=H) and disable (MR2 A13=L) along with Bank and Bank Group Address.

4.10 Post Package Repair (PPR)

For DRAM to operate PPR function independantly on the selected logical rank, logical rank information (C0, C1 and C2) should be given to DRAM at the ACT, WR, WRA, REF and PRE during PPR mode.

In case of PPR with WRA, REF (1x) commands are allowed from PL+WL+BL/2+tWR+tRP after WRA command during tPGM and tPGMPST for proper repair. Upon receiving REF (1x) command, DRAM performs normal Refresh operation and maintains the array content except for the Bank containing row that is being repaired. Other commands except REF during t_{PGM} can cause incomplete repair so no other command except REF to the banks and logical ranks which do not have on-going PPR is allowed during tPGM.

4.11 Gear Down mode

The 3DS device defaults in 1/2 rate(1N) clock mode and utilizes a low frequency MRS command followed by a sync pulse to align the proper clock edge for operating the control lines specifically CS_n, CKE and ODT in 1/4 rate (2N) mode. Only one sync pulse is required for a 3DS device and the sync pulse should be associated with the master die. For operation in 1/2 rate mode the MRS command and sync pulse are not required. For more details on Gear Down mode refer to JESD79-4.

5 On Die Termination

No changes from JESD79-4.

6 Absolute Maximum Ratings

No changes from JESD79-4.

7 AC and DC Operating Conditions

No changes from JESD79-4.

8 AC and DC Output Measurement Levels

No changes from JESD79-4.

9 Speed Bins

9.1 Standard 3DS Speed Bins for x4

Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.

DDR4 3D Stacked SDRAM Standard Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin.

Table 20 — DDR4 x4 3DS-1600 Speed Bins and Operations

Speed Bin			DDR4-1600J-3DS2B		DDR4-1600K-3DS2B		DDR4-1600L-3DS2B		Unit	Note
CL-nRCD-nRP			12-11-10		13-12-11		14-13-12			
Parameter		Symbol	min	max	min	max	min	max		
Internal read command to first data		t_{AA}	15.00	21.5	16.25	21.5	17.50	21.5	ns	
ACT to internal read or write delay time		tRCD	13.75	-	15.00	-	16.25	-	ns	
PRE command period		tRP	12.50	-	13.75	-	15.00	-	ns	
ACT to PRE command period		tRAS	35	9 x tREFI	35	9 x tREFI	35	9 x tREFI	ns	
ACT to ACT or REF command period		tRC	47.50	-	48.75	-	50.00	-	ns	
CWL=9, 11	CL=12	tCK(AVG)	1.25	1.5	Reserved		Reserved		ns	1,2,3,4
	CL-13	tCK(AVG)	1.25	1.5	1.25	1.5	Reserved		ns	1,2,3,4
	CL=14	tCK(AVG)	1.25	1.5	1.25	1.5	1.25	1.5	ns	1,2,3
Supported CL Settings			12,13,14		13, 14		14		nCK	
Supported nRCD Timings minimum			10		10		11		nCK	
Supported nRP Timings minimum			9		10		10		nCK	
Supported CWL Settings			9, 11		9, 11		9, 11		nCK	

9.1 Standard 3DS Speed Bins for x4 (cont'd)

Table 21 — DDR4 x4 3DS-1866 Speed Bins and Operations

Speed Bin			DDR4-1866L-3DS2B		DDR4-1866M-3DS2B		DDR4-1866N-3DS2B		Unit	Note
CL-nRCD-nRP			14-13-12		15-14-13		16-15-14			
Parameter		Symbol	min	max	min	max	min	max		
Internal read command to first data		t_{AA}	15.00	21.5	16.07	21.5	17.14	21.5	ns	
ACT to internal read or write delay time		tRCD	13.92 (13.75[11])	-	15.00	-	16.07	-	ns	
PRE command period		tRP	12.85	-	13.92 (13.75)[13]	-	15.00	-	ns	
ACT to PRE command period		tRAS	34	9 x tREFI	34	9 x tREFI	34	9 x tREFI	ns	
ACT to ACT or REF command period		tRC	46.85	-	47.92	-	49.00	-	ns	
CWL=9, 11	CL=12	tCK(AVG)	1.25	1.5	Reserved		Reserved		ns	1,2,3,4,6
			(Optional)[5]						ns	
	CL=13	tCK(AVG)	1.25	1.5	1.25	1.5	Reserved		ns	1,2,3,4,6
	CL=14	tCK(AVG)	1.25	1.5	1.25	1.5	1.25	1.5	ns	1,2,3,6
CWL=10, 12	CL=14	tCK(AVG)	1.071	< 1.25	Reserved		Reserved		ns	1,2,3,4
	CL=15	tCK(AVG)	1.071	< 1.25	1.071	< 1.25	Reserved		ns	1,2,3,4
	CL=16	tCK(AVG)	1.071	< 1.25	1.071	< 1.25	1.071	< 1.25	ns	1,2,3
Supported CL Settings			12, 13, 14, 15, 16		13, 14, 15, 16		14, 16		nCK	
Supported nRCD Timings minimum			10		10		11		nCK	
Supported nRP Timings minimum			9		10		10		nCK	
Supported CWL Settings			9, 10, 11, 12		9, 10, 11, 12		9, 10, 11, 12		nCK	

9.1 Standard 3DS Speed Bins for x4 (cont'd)

Table 22 — DDR4 x4 3DS-2133 Speed Bins and Operations

Speed Bin			DDR4-2133P-3DS2A		DDR4-2133P-3DS3A		DDR4-2133R-3DS4A		Unit	Note
CL-nRCD-nRP			17-15-15		18-15-15		20-16-16			
Parameter		Symbol	min	max	min	max	min	max		
Internal read command to first data		t_{AA}	15.95	21.5	16.88	21.5	18.76 (17.14)[12]	21.5	ns	
ACT to internal read or write delay time		tRCD	14.06	-	14.06	-	15.00	-	ns	
PRE command period		tRP	14.06 (13.75)[13]	-	14.06	-	15.00	-	ns	
ACT to PRE command period		tRAS	33	9 x tREFI	33	9 x tREFI	33	9 x tREFI	ns	
ACT to ACT or REF command period		tRC	47.06	-	47.06	-	48.00	-	ns	
CWL=9, 11	CL=13	tCK(AVG)	1.25	1.5	Reserved		Reserved		ns	1,2,3,4, 7
	CL=14	tCK(AVG)	1.25	1.5	1.25	1.5	1.25	1.5	ns	1,2,3,7
CWL=10, 12	CL=14	tCK(AVG)	Reserved		Reserved		Reserved		ns	1,2,3, 4,7
	CL=15	tCK(AVG)	1.071	< 1.25	Reserved		Reserved		ns	1,2,3,4, 7
	CL=16	tCK(AVG)	1.071	< 1.25	1.071	< 1.25	1.071	< 1.25	ns	1,2,3,7
CWL=11, 14	CL=16	tCK(AVG)	Reserved		Reserved		Reserved		ns	1,2,3,4
	CL=17	tCK(AVG)	0.937	< 1.071	Reserved		Reserved		ns	1,2,3,4
	CL=18	tCK(AVG)	0.937	< 1.071	0.937	< 1.071	Reserved		ns	1,2,3,4
	CL=20	tCK(AVG)	0.937	< 1.071	0.937	< 1.071	0.937	< 1.071	ns	1,2,3,7
Supported CL Settings			13,14,15,16,17, 18, 20		14, 16, 18		14, 16, 20		nCK	
Supported nRCD Timings minimum			10		10		11		nCK	
Supported nRP Timings minimum			10		10		10		nCK	
Supported CWL Settings			9, 10, 11, 12, 14		9, 10, 11, 12, 14		9, 10, 11, 12, 14		nCK	

Table 23 — DDR4 x4 3DS-2400 Speed Bins and Operations

Speed Bin			DDR4-2400P-3DS3B		DDR4-2400T-3DS2A		DDR4-2400U-3DS2A		DDR4-2400U-3DS4A		Unit	Note
CL-nRCD-nRP			18-16-15		19-17-17		20-18-18		22-18-18			
Parameter		Symbol	min	max	min	max	min	max	min	max		
Internal read command to first data		t_{AA}	15.00	21.50	15.83	21.00	16.67	21.50	18.33 (17.14)[12]	21.50	ns	
ACT to internal read or write delay time		tRCD	13.33	-	14.16	-	15.00	-	15.00	-	ns	
PRE command period		tRP	12.50	-	14.16	-	15.00	-	15.00	-	ns	
ACT to PRE command period		tRAS	32	9 x tREFI	32	9 x tREFI	32	9 x tREFI	32	9 x tREFI	ns	
ACT to ACT or REF command period		tRC	44.50	-	46.16	-	47.00	-	47.00	-	ns	
CWL= 9, 11	CL=13	tCK(AVG)	1.25	1.5	1.25	1.5	Reserved		Reserved		ns	1,2,3,4,8
	CL=14	tCK(AVG)	1.25	1.5	1.25	1.5	1.25	1.5	1.25	1.5	ns	1,2,3,8
CWL= 10, 12	CL=14	tCK(AVG)	1.071	< 1.25	Reserved		Reserved		Reserved		ns	1,2,3,4,8
			(Optional)[5]								ns	1,2,3,4,8
	CL=15	tCK(AVG)	1.071	< 1.25	1.071	1.25	Reserved		Reserved		ns	1,2,3,4,8
	CL=16	tCK(AVG)	1.071	< 1.25	1.071	1.25	1.071	< 1.25	1.071	< 1.25	ns	1,2,3,8
CWL= 11, 14												
	CL=17	tCK(AVG)	0.937	< 1.071	0.937	< 1.071	Reserved		Reserved		ns	1,2,3,4,8
	CL=18	tCK(AVG)	0.937	< 1.071	0.937	< 1.071	0.937	< 1.071	Reserved		ns	1,2,3,4,8
	CL=20	tCK(AVG)	Reserved		Reserved		Reserved		0.937	< 1.071	ns	1,2,3,4,8
CWL= 12, 16	CL=18	tCK(AVG)	0.833	< 0.937	Reserved		Reserved		Reserved		ns	1,2,3,4
	CL=19	tCK(AVG)	0.833	< 0.937	0.833	< 0.937	Reserved		Reserved		ns	1,2,3,4
	CL=20	tCK(AVG)	0.833	< 0.937	0.833	< 0.937	0.833	< 0.937	Reserved		ns	1,2,3,4
	CL=22	tCK(AVG)	Reserved		Reserved		Reserved		0.833	< 0.937	ns	1,2,3,4,8
Supported CL Settings			13, 14, 15, 16, 17,18, 19, 20		13, 14, 15, 16, 17, 18, 19, 20		14, 16, 18, 20		14, 16, 20, 22		nCK	
Supported nRCD Timings minimum			9		10		10		11		nCK	
Supported nRP Timings minimum			9		10		10		10		nCK	
Supported CWL Settings			9, 10, 11, 12, 14, 16		9, 10, 11, 12, 14, 16		9, 10, 11, 12, 14, 16		9, 10, 11, 12, 14, 16		nCK	

9.1 Standard 3DS Speed Bins for x4 (cont'd)

Table 24 — DDR4 x4 3DS-2666 Speed Bins and Operations

Speed Bin			DDR4-2666T- 3DS3A		DDR4-2666V- 3DS3A		DDR4-2666W- 3DS4A		Unit	Note
CL-nRCD-nRP			20-17-17		22-19-19		24-20-20			
Parameter		Symbol	min	max	min	max	min	max		
Internal read command to first data		t_{AA}	15.00	21.50	16.50	21.50	18.00 (17.14)[12]	21.50	ns	
ACT to internal read or write delay time		tRCD	12.75	-	14.25	-	15.00	-	ns	
PRE command period		tRP	12.75	-	14.25	-	15.00	-	ns	
ACT to PRE command period		tRAS	32	9 x tREFI	32	9 x tREFI	32	9 x tREFI	ns	
ACT to ACT or REF command period		tRC	44.75	-	46.25	-	47.00	-	ns	
CWL=9,11	CL=13	tCK(AVG)	1.25	1.5	Reserved		Reserved		ns	1,2,3, 4,9
	CL=14	tCK(AVG)	1.25	1.5	1.25	1.5	1.25	1.5	ns	1,2,3,9
CWL=10,12	CL=14	tCK(AVG)	Reserved		Reserved		Reserved		ns	1,2,3, 4,9
	CL=15	tCK(AVG)	1.071	< 1.25	Reserved		Reserved		ns	1,2,3, 4,9
	CL=16	tCK(AVG)	1.071	< 1.25	1.071	< 1.25	1.071	< 1.25	ns	1,2,3,9
CWL=11,14	CL=16	tCK(AVG)	Reserved		Reserved		Reserved		ns	1,2,3, 4,9
	CL=18	tCK(AVG)	0.937	< 1.071	0.937	< 1.071	Reserved		ns	1,2,3, 4,9
	CL=20	tCK(AVG)	0.937	< 1.071	0.937	< 1.071	0.937	< 1.071	ns	1,2,3,9
CWL=12,16	CL=18	tCK(AVG)	Reserved		Reserved		Reserved		ns	1,2,3, 4,9
	CL=20	tCK(AVG)	0.833	< 0.937	0.833	< 0.937	Reserved		ns	1,2,3, 4,9
	CL=22	tCK(AVG)	0.833	< 0.937	0.833	< 0.937	0.833	< 0.937	ns	1,2,3,9
CWL=14,18	CL=20	tCK(AVG)	0.75	0.833	Reserved		Reserved		ns	1,2,3, 4,9
	CL=22	tCK(AVG)	0.75	0.833	0.75	0.833	Reserved		ns	1,2,3, 4,9
	CL=24	tCK(AVG)	0.75	0.833	0.75	0.833	0.75	0.833	ns	1,2,3,9
Supported CL Settings			13, 14, 15, 16, 18, 20, 22, 24		14, 16, 18, 20, 22, 24		14, 16, 20, 22, 24		nCK	
Supported nRCD Timings minimum			11		12		12		nCK	
Supported nRP Timings minimum			10		12		12		nCK	
Supported CWL Settings			9, 10, 11, 12, 14, 16, 18		9, 10, 11, 12, 14, 16, 18		9, 10, 11, 12, 14, 16, 18		nCK	

Table 25 — DDR4 x4 3DS-3200 Speed Bins and Operations

Speed Bin			DDR4-3200W- 3DS4A		DDR4-3200AA- 3DS4A		DDR4-3200AC- 3DS4A		Unit	Note
CL-nRCD-nRP			24-20-20		26-22-22		28-24-24			
Parameter		Symbol	min	max	min	max	min	max		
Internal read command to first data		t_{AA}	15.00	21.50	16.25	21.50	17.50 (17.14)[12]	21.50	ns	
ACT to internal read or write delay time		tRCD	12.50	-	13.75	-	15.00	-	ns	
PRE command period		tRP	12.50	-	13.75	-	15.00	-	ns	
ACT to PRE command period		tRAS	32	9 x tREFI	32	9 x tREFI	32	9 x tREFI	ns	
ACT to ACT or REF command period		tRC	44.5	-	45.75	-	47.00	-	ns	
CWL=9,11	CL=13	tCK(AVG)	1.25	1.5	Reserved		Reserved		ns	1,2,3,4
	CL=14	tCK(AVG)	1.25	1.5	1.25	1.5	1.25	1.5	ns	1,2,3,10
CWL=10,12	CL=14	tCK(AVG)	Reserved		Reserved		Reserved		ns	1,2,3,4,10
	CL=15	tCK(AVG)	1.071	< 1.25	Reserved		Reserved		ns	1,2,3,4,10
	CL=16	tCK(AVG)	1.071	< 1.25	1.071	< 1.25	1.071	< 1.25	ns	1,2,3,10
CWL=11,14	CL=16	tCK(AVG)	Reserved		Reserved		Reserved		ns	1,2,3,4,10
	CL=18	tCK(AVG)	0.937	< 1.071	0.937	< 1.071	Reserved		ns	1,2,3,4,10
	CL=20	tCK(AVG)	0.937	< 1.071	0.937	< 1.071	0.937	< 1.071	ns	1,2,3,10
CWL=12,16	CL=18	tCK(AVG)	Reserved		Reserved		Reserved		ns	1,2,3,4,10
	CL=20	tCK(AVG)	0.833	< 0.937	0.833	< 0.937	Reserved		ns	1,2,3,4,10
	CL=22	tCK(AVG)	0.833	< 0.937	0.833	< 0.937	0.833	< 0.937	ns	1,2,3,10
CWL=14,18	CL=20	tCK(AVG)	0.75	0.833	Reserved		Reserved		ns	1,2,3,4,10
	CL=22	tCK(AVG)	0.75	0.833	0.75	0.833	Reserved		ns	1,2,3,4,10
	CL=24	tCK(AVG)	0.75	0.833	0.75	0.833	0.75	0.833	ns	1,2,3,10
CWL=16,20	CL=24	tCK(AVG)	0.625	0.75	Reserved		Reserved		ns	1,2,3,10
	CL=26	tCK(AVG)	0.625	0.75	0.625	0.75	Reserved		ns	1,2,3,10
	CL=28	tCK(AVG)	0.625	0.75	0.625	0.75	0.625	0.75	ns	1,2,3,10
Supported CL Settings			13, 14, 15, 16, 18, 20, 22, 24, 26, 28		14, 16, 18, 20, 22, 24, 26, 28		14, 16, 20, 22, 24, 28		nCK	
Supported nRCD Timings minimum			11		12		12		nCK	
Supported nRP Timings minimum			10		11		12		nCK	
Supported CWL Settings			9, 10, 11, 12, 14, 16, 18, 20		9, 10, 11, 12, 14, 16, 18, 20		9, 10, 11, 12, 14, 16, 18, 20		nCK	

9.2 Standard 3DS Speed Bins for x8

x8 speed bins for DDR4 3DS have not been developed at the time of this publication. Users should consult suppliers for specific x8 3DS requirements as timings are not assumed to be inherited from the mono-die specification in JESD79-4.

9.3 Notes to Speed Bin Tables

Absolute Specification

- V_{DDQ} = V_{DD} = 1.20 V +/- 0.06 V
- V_{PP} = 2.5 V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.
- DDR4-3DS-1600, 1866, 2133, 2400 Speed Bin Tables are valid only when Gear Down mode is disabled.

NOTE 1 The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.

NOTE 2 tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (i.e., 1.5 ns or 1.25 ns or 1.071 ns or 0.937 ns or 0.833 ns) when calculating CL [nCK] = t_{AA} [ns] / tCK(avg) [ns], rounding up to the next 'Supported CL', where t_{AA} = 12.5 ns and tCK(avg) = 1.3 ns should only be used for CL = 12 calculation.

NOTE 3 tCK(avg).MAX limits: Calculate tCK(avg) = t_{AA}.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e., 1.5 ns or 1.25 ns or 1.071 ns or 0.937 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.

NOTE 4 'Reserved' settings are not allowed. User must program a different value.

NOTE 5 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.

NOTE 6 Any DDR4-3DS-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

NOTE 7 Any DDR4-3DS-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

NOTE 8 Any DDR4-3DS-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

NOTE 9 Any DDR4-3DS-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

NOTE 10 Any DDR4-3DS-3200 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

NOTE 11 13.75 ns is minimum tRCD when operating by DDR4-1600J-3DS2B at tCK(AVG).min=1.25 ns.

NOTE 12 17.14 ns is the minimum t_{AA} when operating in DDR4-1866N-3DS2B at tCK(AVG).min=1.071 ns.

NOTE 13 13.75 ns is minimum tRP when operating by DDR4-1600K-3DS2B at tCK(AVG).min=1.25 ns.

10 I_{DD} Current Specification

10.1 I_{DD}, I_{PP}, and I_{DDQ} Measurement Conditions

In this chapter, I_{DD}, I_{PP}, and I_{DDQ} measurement conditions such as test load and patterns are defined. Figure 7 shows the setup and test load for I_{DD}, I_{PP} and I_{DDQ} measurements.

I_{DD} currents (such as I_{DD0}, I_{DD0A}, I_{DD1}, I_{DD1A}, I_{DD2N}, I_{DD2NA}, I_{DD2NL}, I_{DD2NT}, I_{DD2P}, I_{DD2Q}, I_{DD3N}, I_{DD3NA}, I_{DD3P}, I_{DD4R}, I_{DD4W}, I_{DD5B1}, I_{DD5B2}, I_{DD5F2}, I_{DD5F4}, I_{DD6N}, I_{DD6E}, I_{DD6R}, I_{DD6A}, I_{DD7}, and I_{DD8}) are measured as time-averaged currents with all V_{DD} balls of the DDR4 SDRAM under test tied together. Any I_{DDQ} current is not included in I_{DD} currents.

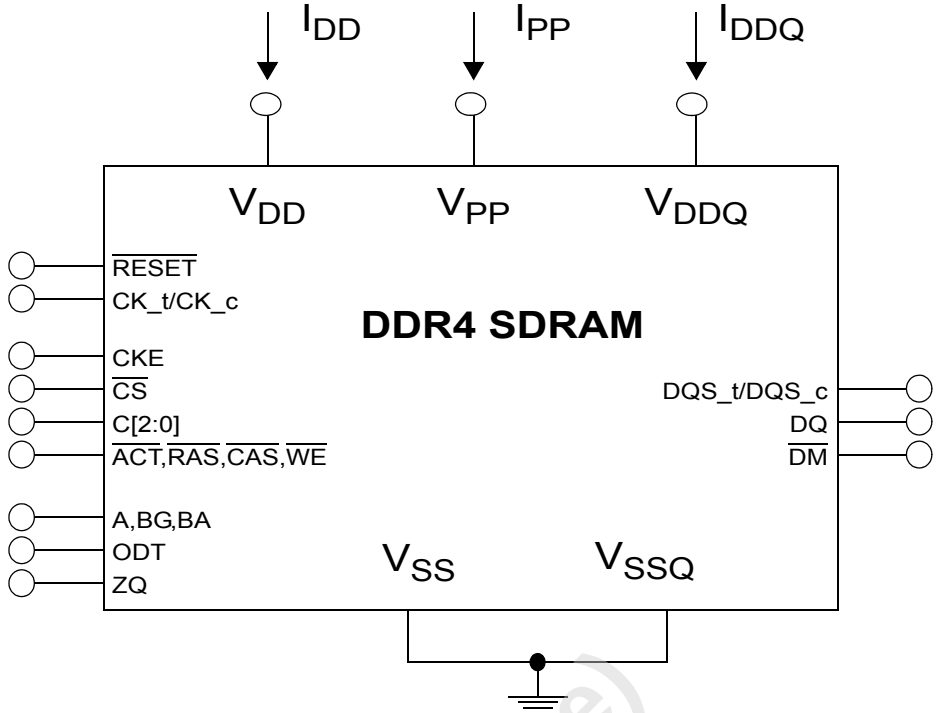
I_{PP} currents have the same definition as I_{DD} except that the current on the V_{PP} supply is measured.

I_{DDQ} currents (such as I_{DDQ2NT} and I_{DDQ4R}) are measured as time-averaged currents with all V_{DDQ} balls of the DDR4 SDRAM under test tied together. Any I_{DD} current is not included in I_{DDQ} currents.
Attention: I_{DDQ} values cannot be directly used to calculate IO power of the DDR4 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 8. In SDRAM module application, I_{DDQ} cannot be measured separately since V_{DD} and V_{DDQ} are using one merged-power layer in Module PCB.

For I_{DD} and I_{DDQ} measurements, the following definitions apply:

- "0" and "LOW" is defined as VIN <= $V_{IL(AC)max}$.
- "1" and "HIGH" is defined as VIN >= $V_{IH(AC)min}$.
- "MID-LEVEL" is defined as inputs are VREF = V_{DD} / 2.
- Timings used for I_{DD} and I_{DDQ} Measurement-Loop Patterns are provided in Table 26.
- Basic I_{DD}, I_{PP} and I_{DDQ} Measurement Conditions are described in Table 27.
- I_{DD} Measurements are done after properly initializing the DDR4 SDRAM. This includes but is not limited to setting:
  RON = RZQ/7 (34 Ohm in MR1);
  Qoff = 0_B (Output Buffer enabled in MR1);
  R_{TT}_NOM = RZQ/6 (40 Ohm in MR1);
  R_{TT}_WR = RZQ/2 (120 Ohm in MR2);
  R_{TT}_PARK = Disable;
  Qoff = 0_B (Output Buffer enabled) in MR1;
  TDQS_t Feature disabled in MR1;
  CRC disabled in MR2;
  CA parity feature disabled in MR5;
  Gear Down mode disabled in MR3.
- **Attention:** The I_{DD}, I_{PP} and I_{DDQ} Measurement-Loop Patterns need to be executed at least one time before actual I_{DD}, I_{PP} or I_{DDQ} measurement is started.
- Define D = {CS0_n, , ACT_n, RAS_n, CAS_n, WE_n } := {HIGH,, LOW, LOW, LOW, LOW}
- Define D# = {CS0_n, , ACT_n, RAS_n, CAS_n, WE_n } := {HIGH, HIGH, HIGH, HIGH, HIGH}

10.1 I_{DD}, I_{PP}, and I_{DDQ} Measurement Conditions (cont'd)



NOTE 1 DIMM level Output test load condition may be different.

Figure 7 — Measurement Setup and Test Load for I_{DD} and I_{DDQ} (optional) Measurements

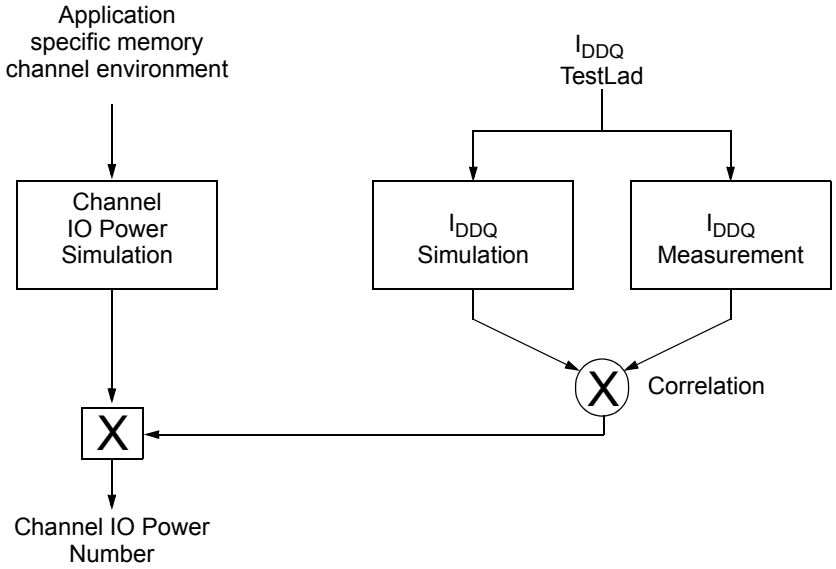


Figure 8 — Correlation from simulated Channel I/O Power to actual Channel I/O Power supported by I_{DDQ} Measurement

10.1 I_{DD}, I_{PP}, and I_{DDQ} Measurement Conditions (cont'd)

Table 26 — Timings used for I_{DD}, I_{PP}, and I_{DDQ} measurements loop patterns

Symbol		DDR4-1600			DDR4-1866			Unit
		12-11-10	13-12-11	14-13-12	14-13-12	15-14-13	16-15-14	
tCK		1.25			1.07			ns
CL		12	13	14	14	15	16	nCK
CWL		11			12			nCK
nRCD		11	12	13	13	14	15	nCK
nRC		38	39	40	44	45	46	nCK
nRAS		28			32			nCK
nRP		10	11	12	12	13	14	nCK
nFAW_slr	x4	16			16			nCK
	x8	20			22			nCK
nRRD_S_slr	x4	4			4			nCK
	x8	4			4			nCK
nRRD_L_slr	x4	5			5			nCK
	x8	5			5			nCK
nRFC_slr 4 Gb		208			243			nCK
nRFC_slr 8 Gb		280			328			nCK
nRFC_slr 16 Gb		TBD			TBD			nCK
nRFC_dlr 4 Gb		72			85			nCK
nRFC_dlr 8 Gb		96			113			nCK
nRFC_dlr 16 Gb		TBD			TBD			nCK

Symbol		DDR4-2133			DDR4-2400			Unit
		16-15-14	18-16-16	20-16-16	18-16-15	20-18-18	22-18-18	
t_{CK}		0.935			0.833			ns
CL		16	18	20	18	20	22	nCK
CWL		14			16			nCK
nRCD		15	16	16	16	18	18	nCK
nRC		50	52	52	54	57	57	nCK
nRAS		36			39			nCK
nRP		14	16	16	15	18	18	nCK
nFAW_slr	x4	16			16			nCK
	x8	23			26			nCK
nRRD_S_slr	x4	4			4			nCK
	x8	4			4			nCK
nRRD_L_slr	x4	6			6			nCK
	x8	6			6			nCK
nRFC_slr 4 Gb		278			312			nCK
nRFC_slr 8 Gb		375			420			nCK
nRFC_slr 16 Gb		TBD			TBD			nCK
nRFC_dlr 4 Gb		97			108			nCK
nRFC_dlr 8 Gb		129			144			nCK
nRFC_dlr 16 Gb		TBD			TBD			nCK

10.1 I_{DD}, I_{PP}, and I_{DDQ} Measurement Conditions (cont'd)

Table 27 defines 3DS I_{DD} definition per 3DS package.

Table 27 — Basic I_{DD}, I_{PP}, and I_{DDQ} Measurement Conditions

Symbol	Description
I_{DD0}	**Operating One Bank Active-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, CL**: see Table 26; **BL:** 8[1]; **AL:** 0; **CS_n:** High between ACT and PRE; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 28; **Data IO:** V_{DDQ}; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 28); L**ogical Rank Activity**: Cycling with one logical rank active at a time; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 28
I_{DD0A}	**Operating One Bank Active-Precharge Current (AL=CL-2)** **AL = CL-2, Other conditions:** see I_{DD0}
I_{PP0}	**Operating One Bank Active-Precharge I_{PP} Current** **Same condition with I_{DD0}**
I_{DD1}	**Operating One Bank Active-Read-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, CL**: see Table 26; **BL:** 8[1]; **AL:** 0; **CS_n**: High between ACT, RD and PRE; **Command, Address, Bank Group Address, Bank Address Inputs, Data IO:** partially toggling according to Table 29; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 29); L**ogical Rank Activity**: Cycling with one ogical rank active at a time; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 29
I_{DD1A}	**Operating One Bank Active-Read-Precharge Current (AL=CL-2)** **AL = CL-2, Other conditions:** see I_{DD1}
I_{PP1}	**Operating One Bank Active-Read-Precharge I_{PP} Current** **Same condition with I_{DD1}**
I_{DD2N}	**Precharge Standby Current (AL=0)** **CKE**: High; **External clock:** On; **tCK, CL**: see Table 26; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 30; **Data IO:** V_{DDQ}; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 30
I_{DD2NA}	**Precharge Standby Current (AL=CL-2)** **AL = CL-2, Other conditions:** see I_{DD2N}
I_{PP2N}	**Precharge Standby I_{PP} Current** **Same condition with I_{DD2N}**
I_{DD2NT}	**Precharge Standby ODT Current** **CKE**: High; **External clock:** On; **tCK, CL**: see Table 26; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 31; **Data IO:** V_{SSQ}; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** toggling according to Table 31; **Pattern Details:** see Table 31
I_{DDQ2NT} (Optional)	**Precharge Standby ODT I_{DDQ} Current** Same definition like for I_{DD2NT}, however measuring I_{DDQ} current instead of I_{DD} current
I_{DD2NL}	**Precharge Standby Current with CAL enabled** Same definition like for I_{DD2N}, CAL enabled[3]
I_{DD2NG}	**Precharge Standby Current with Gear Down mode enabled** Same definition like for I_{DD2N}, Gear Down mode enabled[3]
I_{DD2ND}	**Precharge Standby Current with DLL disabled** Same definition like for I_{DD2N}, DLL disabled[3]

I_{DD2N_par}	**Precharge Standby Current with CA parity enabled** Same definition like for I_{DD2N}, CA parity enabled[3]
I_{DD2P}	**Precharge Power-Down Current CKE:** Low; **External clock:** On; **tCK, CL**: see Table 26; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** V_{DDQ}; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
I_{PP2P}	**Precharge Power-Down I_{PP} Current** **Same condition with I_{DD2P}**
I_{DD2Q}	**Precharge Quiet Standby Current** **CKE**: High; **External clock:** On; **tCK, CL**: see Table 26; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** V_{DDQ}; **DM_n:** stable at 1;**Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
I_{DD3N}	**Active Standby Current** **CKE**: High; **External clock:** On; **tCK, CL**: see Table 26; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 30; **Data IO:** V_{DDQ}; **DM_n:** stable at 1;**Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 30
I_{DD3NA}	**Active Standby Current (AL=CL-2)** **AL = CL-2, Other conditions:** see I_{DD3N}
I_{PP3N}	**Active Standby I_{PP} Current** **Same condition with I_{DD3N}**
I_{DD3P}	**Active Power-Down Current** **CKE:** Low; **External clock:** On; **tCK, CL**: see Table 26; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** V_{DDQ}; **DM_n:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
I_{PP3P}	**Active Power-Down IPP Current** **Same condition with IDD3P**
I_{DD4R}	**Operating Burst Read Current** **CKE:** High; **External clock:** On; **tCK, CL**: see Table 26; **BL:** 8[2]; **AL:** 0; **CS_n**: High between RD; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 32; **Data IO:** seamless read data burst with different data between one burst and the next one according to Table 32; **DM_n**: stable at 1; **Bank Activity:** all banks of all logical ranks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 32) and through logical ranks; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 32
I_{DD4RA}	**Operating Burst Read Current (AL=CL-2)** **AL = CL-2, Other conditions:** see I_{DD4R}
I_{PP4R}	**Operating Burst Read I_{PP} Current** **Same condition with I_{DD4R}**
I_{DDQ4R} (Optional)	**Operating Burst Read I_{DDQ} Current** Same definition like for I_{DD4R}, however measuring I_{DDQ} current instead of I_{DD} current
I_{DD4W}	**Operating Burst Write Current** **CKE:** High; **External clock:** On; **tCK, CL**: see Table 26; **BL:** 8[1]; **AL:** 0; **CS_n**: High between WR; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 33; **Data IO:** seamless write data burst with different data between one burst and the next one according to Table 33; **DM_n:** stable at 1; **Bank Activity:** all banks open of all logical ranks, WR commands cycling through banks: 0,0,1,1,2,2,... (see Table 33) and through logical ranks; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at HIGH; **Pattern Details:** see Table 33
I_{DD4WA}	**Operating Burst Write Current (AL=CL-2)** **AL = CL-2, Other conditions:** see I_{DD4W}
I_{DD4WC}	**Operating Burst Write Current with Write CRC** **Write CRC enabled[3], Other conditions:** see I_{DD4W}
I_{DD4W_par}	**Operating Burst Write Current with CA Parity** **CA Parity enabled[3], Other conditions:** see I_{DD4W}

I_{PP4W}	**Operating Burst Write I_{PP} Current** **Same condition with I_{DD4W}**
I_{DD5B1}	**Burst Refresh Current (1X REF)** **CKE:** High; **External clock:** On; **tCK, CL, nRFC**: see Table 26; **BL:** 8[1]; **AL:** 0; **CS_n**: High between REF; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 34; **Data IO:** V_{DDQ}; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFC (see Table 34); L**ogical Rank Activity**: REF command staggered nRFC_dlr between REF command to REF command; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 34
I_{PP5B1}	**Burst Refresh Write I_{PP} Current (1X REF)** **Same condition with I_{DD5B1}**
I_{DD5B2}	**Burst Refresh Current (1X REF)** **CKE:** High; **External clock:** On; **tCK, CL, nRFC**: see Table 26; **BL:** 8[1]; **AL:** 0; **CS_n**: High between REF; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 34; **Data IO:** V_{DDQ}; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFC (see Table 34); L**ogical Rank Activity**: REF command staggered nRFC_slr between REF command to REF command; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 34
I_{PP5B2}	**Burst Refresh Write I_{PP} Current (1X REF)** **Same condition with I_{DD5B2}**
I_{DD5F2}	**Burst Refresh Current (2X REF)** **tRFC=tRFC_x2, Other conditions:** see I_{DD5B1}
I_{PP5F2}	**Burst Refresh Write I_{PP} Current (2X REF)** **Same condition with I_{DD5F2}**
I_{DD5F3}	**Burst Refresh Current (2X REF)** **tRFC=tRFC_x2, Other conditions:** see I_{DD5B2}
I_{PP5F3}	**Burst Refresh Write I_{PP} Current (2X REF)** **Same condition with I_{DD5F3}**
I_{DD5F4}	**Burst Refresh Current (4X REF)** **tRFC=tRFC_x4, Other conditions:** see I_{DD5B1}
I_{PP5F4}	**Burst Refresh Write I_{PP} Current (4X REF)** **Same condition with I_{DD5F4}**
I_{DD5F5}	**Burst Refresh Current (4X REF)** **tRFC=tRFC_x4, Other conditions:** see I_{DD5B2}
I_{PP5F5}	**Burst Refresh Write I_{PP} Current (4X REF)** **Same condition with I_{DD5F5}**
I_{DD6N}	**Self Refresh Current: Normal Temperature Range** ***T_{CASE}*: 0 - 85°C; Low Power Array Self Refresh (LP ASR)** : Normal[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c: LOW; **CL**: see Table 26; **BL:** 8[1]; **AL:** 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n:** stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
I_{PP6N}	**Self Refresh I_{PP} Current: Normal Temperature Range** **Same condition with I_{DD6N}**
I_{DD6E}	**Self-Refresh Current: Extended Temperature Range**) ***T_{CASE}*: 0 - 95°C; Low Power Array Self Refresh (LP ASR)** : Extended[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c: LOW; **CL**: see Table 26; **BL:** 8[1]; **AL:** 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LE**VEL**
I_{PP6E}	**Self Refresh I_{PP} Current: Extended Temperature Range** **Same condition with I_{DD6E}**
I_{DD6R}	**Self-Refresh Current: Reduced Temperature Range** ***T_{CASE}*: 0 - TBD (~35-45)°C; Low Power Array Self Refresh (LP ASR)** : Reduced[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c: LOW; **CL**: see Table 26; **BL:** 8[1]; **AL:** 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL

I_{PP6R}	**Self Refresh I_{PP} Current: Reduced Temperature Range** **Same condition with I_{DD6R}**
I_{DD6A}	**Auto Self-Refresh Current** ***T_{CASE}*: 0 - 95°C; **Low Power Array Self Refresh (LP ASR)** : Auto[4];**Partial Array Self-Refresh (PASR)**: Full Array; **CKE:** Low; **External clock:** Off; CK_t and CK_c: LOW; **CL**: see Table 26; **BL:** 8[1]; **AL:** 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Auto Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
I_{PP6A}	**Auto Self-Refresh I_{PP} Current** **Same condition with I_{DD6A}**
I_{DD7}	**Operating Bank Interleave Read Current** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL**: see Table 26; **BL:** 8[1]; **AL:** CL-2; **CS_n**: High between ACT and RDA; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 37; **Data IO:** read data bursts with different data between one burst and the next one according to Table 37; **DM_n:** stable at 1; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing, see Table 35; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 35
I_{PP7}	**Operating Bank Interleave Read I_{PP} Current** **Same condition with I_{DD7}**
I_{DD8}	**Maximum Power Down Current** **TBD**
I_{PP8}	**Maximum Power Down I_{PP} Current** **Same condition with I_{DD8}**

NOTE 1 Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].

NOTE 2 Output Buffer Enable
- set MR1 [A12 = 0] : Qoff = Output buffer enabled
- set MR1 [A2:1 = 00] : Output Driver Impedance Control = RZQ/7

RTT_Nom enable
- set MR1 [A10:8 = 011] : RTT_NOM = RZQ/6

RTT_WR enable
- set MR2 [A10:9 = 01] : RTT_WR = RZQ/2

RTT_PARK disable
- set MR5 [A8:6 = 000]

NOTE 3 CAL enabled : set MR4 [A8:6 = 001] : 1600MT/s
010] : 1866MT/s, 2133MT/s
011] : 2400MT/s

Gear Down mode enabled :set MR3 [A3 = 1] : 1/4 Rate

DLL disabled : set MR1 [A0 = 0]

CA parity enabled :set MR5 [A2:0 = 001] : 1600MT/s,1866MT/s, 2133MT/s
010] : 2400MT/s

NOTE 4 Low Power Array Self Refresh (LP ASR) : set MR2 [A7:6 = 00] : Normal
01] : Reduced Temperature range
10] : Extended Temperature range
11] : Auto Self Refresh

10.1 I_{DD}, I_{PP}, and I_{DDQ} Measurement Conditions (cont'd)

Table 28 — I_{DD0}, I_{DD0A} and I_{PP0} Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Logical Rank-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/ A16	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][2]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	0	**ACT**	0	0	0	0	0	0	000	0	0	0	0	0	0	0	0	-
				1,2	D, D	1	0	0	0	0	0	000	0	0	0	0	0	0	0	0	-
				3,4	D_#, D_#	1	1	1	1	1	0	000	3	3	0	0	0	7	F	0	-
				...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
				nRAS	PRE	0	1	0	1	0	0	000	0	0	0	0	0	0	0	0	-
				...	repeat pattern 1...4 until nRC - 1, truncate if necessary																
			1	1*nRC	repeat Logical Rank-loop 0, use C[2:0][2] = 001 instead																
			2	2*nRC	repeat Logical Rank-loop 0, use C[2:0][2] = 010 instead																
			3	3*nRC	repeat Logical Rank-loop 0, use C[2:0][2] = 011 instead																
			4	4*nRC	repeat Logical Rank-loop 0, use C[2:0][2] = 100 instead																
			5	5*nRC	repeat Logical Rank-loop 0, use C[2:0][2] = 101 instead																
			6	6*nRC	repeat Logical Rank-loop 0, use C[2:0][2] = 110 instead																
			7	7*nRC	repeat Logical Rank-loop 0, use C[2:0][2] = 111 instead																
		1		8*nRC	repeat Sub-Loop 0, use **BG[1:0] = 1, BA[1:0] = 1** instead																
		2		16*nRC	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 2** instead																
		3		24*nRC	repeat Sub-Loop 0, use **BG[1:0] = 1, BA[1:0] = 3** instead																
		4		32*nRC	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 1** instead																
		5		40*nRC	repeat Sub-Loop 0, use **BG[1:0] = 1, BA[1:0] = 2** instead																
		6		48*nRC	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 3** instead																
		7		56*nRC	repeat Sub-Loop 0, use **BG[1:0] = 1, BA[1:0] = 0** instead																
		8		64*nRC	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 0** instead																
		9		72*nRC	repeat Sub-Loop 0, use **BG[1:0] = 3, BA[1:0] = 1** instead																
		10		80*nRC	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 2** instead																
		11		88*nRC	repeat Sub-Loop 0, use **BG[1:0] = 3, BA[1:0] = 3** instead																
		12		96*nRC	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 1** instead																
		13		104*nRC	repeat Sub-Loop 0, use **BG[1:0] = 3, BA[1:0] = 2** instead																
		14		112*nRC	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 3** instead																
		15		120*nRC	repeat Sub-Loop 0, use **BG[1:0] = 3, BA[1:0] = 0** instead																

NOTE 1 DQS_t, DQS_c are V_{DDQ}.
NOTE 2 C2 is a don't care for 2H and 4H 3DS devices. C1 is a don't care for 2H 3DS devices.
NOTE 3 DQ signals are V_{DDQ}.

Table 29 — I_{DD1}, I_{DD1A} and I_{PP1} Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Logical Rank-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][2]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	0	**ACT**	0	0	0	0	0	0	000	0	**0**	**0**	0	0	0	0	0	-
				1, 2	D, D	1	0	0	0	0	0	000	0	**0**	**0**	0	0	0	0	0	-
				3, 4	D#, D#	1	1	1	1	1	0	000	3	**3**	**0**	0	0	7	F	0	-
				...	repeat pattern 1...4 until nRCD - AL - 1, truncate if necessary																
				nRCD -AL	**RD**	0	1	1	0	1	0	000	0	0	0	0	0	0	0	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
				...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
				nRAS	**PRE**	0	1	0	1	0	0	000	0	**0**	**0**	0	0	0	0	0	-
				...	repeat pattern 1...4 until nRC - 1, truncate if necessary																
			1	1*nRC	repeat Logical Rank-loop 0, use C[2:0][2] = 001 instead																
			2	2*nRC	repeat Logical Rank-loop 0, use C[2:0][2] = 010 instead																
			3	3*nRC	repeat Logical Rank-loop 0, use C[2:0][2] = 011 instead																
			4	4*nRC	repeat Logical Rank-loop 0, use C[2:0][2] = 100 instead																
			5	5*nRC	repeat Logical Rank-loop 0, use C[2:0][2] = 101 instead																
			6	6*nRC	repeat Logical Rank-loop 0, use C[2:0][2] = 110 instead																
			7	7*nRC	repeat Logical Rank-loop 0, use C[2:0][2] = 111 instead																
		1	0	8*nRC + 0	**ACT**	0	0	0	1	1	0	000	1	**1**	**0**	0	0	0	0	0	-
				8*nRC + 1, 2	D, D	1	0	0	0	0	0	**000**	**0**	0	0	0	0	0	0	0	-
				8*nRC + 3, 4	D#, D#	1	1	1	1	1	0	**000**	3[b]	**3**	**0**	0	0	7	F	0	-
				...	repeat pattern nRC + 1...4 until 1*nRC + nRAS - 1, truncate if necessary																
				8*nRC + nRCD - AL	**RD**	0	1	1	0	1	0	**000**	**1**	1	0	0	0	0	**0**	**0**	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
				...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
				8*nRC + nRAS	**PRE**	0	1	0	1	0	0	000	0	**0**	**0**	0	0	0	0	0	-
				...	repeat nRC + 1...4 until 2*nRC - 1, truncate if necessary																
			1	9*nRC	repeat Logical Rank-loop 0, use C[2:0][2] = 001 instead																
			2	10*nRC	repeat Logical Rank-loop 0, use C[2:0][2] = 010 instead																
			3	11*nRC	repeat Logical Rank-loop 0, use C[2:0][2] = 011 instead																
			4	12*nRC	repeat Logical Rank-loop 0, use C[2:0][2] = 100 instead																
			5	13*nRC	repeat Logical Rank-loop 0, use C[2:0][2] = 101 instead																
			6	14*nRC	repeat Logical Rank-loop 0, use C[2:0][2] = 110 instead																
			7	15*nRC	repeat Logical Rank-loop 0, use C[2:0][2] = 111 instead																
		2		16*nRC	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 2** instead																
		3		24*nRC	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 3** instead																
		4		32*nRC	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 1** instead																

Table 29 — I_{DD1}, I_{DD1A} and I_{PP1} Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Logical Rank-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][2]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
		5		40*nRC	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 2** instead																
		6		48*nRC	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 3** instead																
		7		56*nRC	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 0** instead																
		8		64*nRC	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 0** instead																
		9		72*nRC	repeat Sub-Loop 1, use **BG[1:0] = 2, BA[1:0] = 1** instead																
		10		80*nRC	repeat Sub-Loop 0, use **BG[1:0] = 3, BA[1:0] = 2** instead																
		11		88*nRC	repeat Sub-Loop 1, use **BG[1:0] = 2, BA[1:0] = 3** instead																
		12		96*nRC	repeat Sub-Loop 0, use **BG[1:0] = 3, BA[1:0] = 1** instead																
		13		104*nRC	repeat Sub-Loop 1, use **BG[1:0] = 2, BA[1:0] = 2** instead																
		14		112*nRC	repeat Sub-Loop 0, use **BG[1:0] = 3, BA[1:0] =** 3 instead																
		15		120*nRC	repeat Sub-Loop 1, use **BG[1:0] = 2, BA[1:0] =** 0 instead																

NOTE 1 DQS_t, DQS_c are used according to RD Commands, otherwise V_{DDQ}.

NOTE 2 C2 is a don't care for 2H and 4H 3DS devices. C1 is a don't care for 2H 3DS devices.

NOTE 3 Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are V_{DDQ}.

Table 30 — I_{DD2N}, I_{DD2NA}, I_{DD2NL}, I_{DD2NG}, I_{DD2ND}, I_{DD2N_par}, I_{PP2}, I_{DD3N}, I_{DD3NA}, and I_{DD3P} Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][2]	BG[1:0]2	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	D, D	1	0	0	0	0	0	000	**0**	**0**	0	0	0	**0**	**0**	0	0
			1	D, D	1	0	0	0	0	0	000	**0**	**0**	0	0	0	**0**	**0**	0	0
			2	D#, D#	1	1	1	1	1	0	000	**3**	**3**	0	0	0	**7**	**F**	0	0
			3	D#, D#	1	1	1	1	1	0	000	**3**	**3**	0	0	0	**7**	**F**	0	0
		1	4-7	repeat Sub-Loop 0, use **BG[1:0] = 1, BA[1:0] = 1** instead																
		2	8-11	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 2** instead																
		3	12-15	repeat Sub-Loop 0, use **BG[1:0] = 1, BA[1:0] = 3** instead																
		4	16-19	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 1** instead																
		5	20-23	repeat Sub-Loop 0, use **BG[1:0] = 1, BA[1:0] = 2** instead																
		6	24-27	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 3** instead																
		7	28-31	repeat Sub-Loop 0, use **BG[1:0] = 1, BA[1:0] = 0** instead																
		8	32-35	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 0** instead																
		9	36-39	repeat Sub-Loop 0, use **BG[1:0] = 3, BA[1:0] = 1** instead																
		10	40-43	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 2** instead																
		11	44-47	repeat Sub-Loop 0, use **BG[1:0] = 3, BA[1:0] = 3** instead																
		12	48-51	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 1** instead																
		13	52-55	repeat Sub-Loop 0, use **BG[1:0] = 3, BA[1:0] = 2** instead																
		14	56-59	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 3** instead																
		15	60-63	repeat Sub-Loop 0, use **BG[1:0] = 3, BA[1:0] = 0** instead																

NOTE 1 DQS_t, DQS_c are V_{DDQ}.

NOTE 2 C2 is a don't care for 2H and 4H 3DS devices. C1 is a don't care for 2H 3DS devices.

NOTE 3 DQ signals are V_{DDQ}.

Table 31 — I_{DD2NT} and I_{DDQ2NT} Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][2]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	D, D	1	0	0	0	0	0	000	**0**	**0**	0	0	0	**0**	**0**	0	-
			1	D, D	1	0	0	0	0	0	000	**0**	**0**	0	0	0	**0**	**0**	0	-
			2	D#, D#	1	1	1	1	1	0	000	**3**	**3**	0	0	0	**7**	**F**	0	-
			3	D#, D#	1	1	1	1	1	0	000	**3**	**3**	0	0	0	**7**	**F**	0	-
		1	4-7	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0] = 1, BA[1:0] = 1** instead																
		2	8-11	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0] = 0, BA[1:0] = 2** instead																
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0] = 1, BA[1:0] = 3** instead																
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0] = 0, BA[1:0] = 1** instead																
		5	20-23	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0] = 1, BA[1:0] = 2** instead																
		6	24-27	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0] = 0, BA[1:0] = 3** instead																
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0] = 1, BA[1:0] = 0** instead																
		8	32-35	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0] = 2, BA[1:0] = 0** instead																
		9	36-39	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0] = 3, BA[1:0] = 1** instead																
		10	40-43	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0] = 2, BA[1:0] = 2** instead																
		11	44-47	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0] = 3, BA[1:0] = 3** instead																
		12	48-51	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0] = 2, BA[1:0] = 1** instead																
		13	52-55	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0] = 3, BA[1:0] = 2** instead																
		14	56-59	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0] = 2, BA[1:0] = 3** instead																
		15	60-63	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0] = 3, BA[1:0] = 0** instead																

NOTE 1 DQS_t, DQS_c are V_{DDQ}.
NOTE 2 C2 is a don't care for 2H and 4H 3DS devices. C1 is a don't care for 2H 3DS devices.
NOTE 3 DQ signals are V_{DDQ}.

Table 32 — I_{DD4R}, I_{DDR4RA} and I_{DDQ4R} Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Logical Rank Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][2]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	0	**RD**	0	1	1	0	1	0	000	**0**	**0**	0	0	0	**0**	**0**	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
				1	D	1	0	0	0	0	0	000	**0**	**0**	0	0	0	**0**	**0**	0	-
				2,3	D#, D#	1	1	1	1	1	0	000	**3**	**3**	0	0	0	**7**	**F**	0	-
		1		4	**RD**	0	1	1	0	1	0	000	**1**	**1**	0	0	0	**7**	**F**	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
				5	D	1	0	0	0	0	0	000	**0**	**0**	0	0	0	**0**	**0**	0	-
				6,7	D#, D#	1	1	1	1	1	0	000	**3**	**3**	0	0	0	**7**	**F**	0	-
		2		8-11	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 2** instead																
		3		12-15	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 3** instead																
		4		16-19	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 1** instead																
		5		20-23	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 2** instead																
		6		24-27	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 3** instead																
		7		28-31	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 0** instead																
		8		32-35	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 0** instead																
		9		36-39	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 1** instead																
		10		40-43	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 2** instead																
		11		44-47	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 3** instead																
		12		48-51	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 1** instead																
		13		52-55	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 2** instead																
		14		56-59	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 3** instead																
		15		60-63	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 0** instead																
			1	64-127	repeat Logical Rank-loop 0, use C[2:0][2] = 001 instead																
			2	128-191	repeat Logical Rank-loop 0, use C[2:0][2] = 010 instead																
			3	192-255	repeat Logical Rank-loop 0, use C[2:0][2] = 011 instead																
			4	256-319	repeat Logical Rank-loop 0, use C[2:0][2] = 100 instead																
			5	320-383	repeat Logical Rank-loop 0, use C[2:0][2] = 101 instead																
			6	384-447	repeat Logical Rank-loop 0, use C[2:0][2] = 110 instead																
			7	448-511	repeat Logical Rank-loop 0, use C[2:0][2] = 111 instead																

NOTE 1 DQS_t, DQS_c are used according to RD Commands, otherwise V_{DDQ}.
NOTE 2 C2 is a don't care for 2H and 4H 3DS devices. C1 is a don't care for 2H 3DS devices.
NOTE 3 Burst Sequence driven on each DQ signal by Read Command.

Table 33 — I_{DD4W}, I_{DD4WA} and I_{DD4W_par} Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Logical Rank Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][2]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	0	**WR**	0	1	1	0	0	0	000	**0**	**0**	0	0	0	**0**	**0**	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
				1	D	1	0	0	0	0	0	000	**0**	**0**	0	0	0	**0**	**0**	0	-
				2,3	D#, D#	1	1	1	1	1	0	000	**3**	**3**	0	0	0	**7**	**F**	0	-
		1		4	**WR**	0	1	1	0	0	0	000	**1**	**1**	0	0	0	**7**	**F**	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
				5	D	1	0	0	0	0	0	000	**0**	**0**	0	0	0	**0**	**0**	0	-
				6,7	D#, D#	1	1	1	1	1	0	000	**3**	**3**	0	0	0	**7**	**F**	0	-
		2		8-11	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 2** instead																
		3		12-15	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 3** instead																
		4		16-19	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 1** instead																
		5		20-23	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 2** instead																
		6		24-27	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 3** instead																
		7		28-31	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 0** instead																
		8		32-35	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 0** instead																
		9		36-39	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 1** instead																
		10		40-43	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 2** instead																
		11		44-47	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 3** instead																
		12		48-51	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 1** instead																
		13		52-55	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 2** instead																
		14		56-59	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 3** instead																
		15		60-63	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 0** instead																
			1	64-127	repeat Logical Rank-loop 0, use C[2:0][2] = 001 instead																
			2	128-191	repeat Logical Rank-loop 0, use C[2:0][2] = 010 instead																
			3	192-255	repeat Logical Rank-loop 0, use C[2:0][2] = 011 instead																
			4	256-319	repeat Logical Rank-loop 0, use C[2:0][2] = 100 instead																
			5	320-383	repeat Logical Rank-loop 0, use C[2:0][2] = 101 instead																
			6	384-447	repeat Logical Rank-loop 0, use C[2:0][2] = 110 instead																
			7	448-511	repeat Logical Rank-loop 0, use C[2:0][2] = 111 instead																

NOTE 1 DQS_t, DQS_c are used according to WR Commands, otherwise V_{DDQ}.
NOTE 2 C2 is a don't care for 2H and 4H 3DS devices. C1 is a don't care for 2H 3DS devices.
NOTE 3 Burst Sequence driven on each DQ signal by Write Command.

Table 34 — I_{DD4WC} Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][2]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	**WR**	0	1	1	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF D8=CRC**
			1,2	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			3,4	D#, D#	1	1	1	1	1	0	0	**3**	**3**	0	0	0	**7**	**F**	0	-
			5	**WR**	0	1	1	0	0	0	0	**1**	**1**	0	0	0	**7**	**F**	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 D8=CRC**
			6,7	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			8,9	D#, D#	1	1	1	1	1	0	0	**3**	**3**	0	0	0	**7**	**F**	0	-
		2	10-14	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 2** instead																
		3	15-19	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 3** instead																
		4	20-24	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 1** instead																
		5	25-29	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 2** instead																
		6	30-34	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 3** instead																
		7	35-39	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 0** instead																
		8	40-44	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 0** instead																
		9	45-49	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 1** instead																
		10	50-54	repeat Sub-Loop 0, use **BG[1:0[2] = 2, BA[1:0] = 2** instead																
		11	55-59	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 3** instead																
		12	60-64	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 1** instead																
		13	65-69	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 2** instead																
		14	70-74	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 3** instead																
		15	75-79	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 0** instead																

NOTE 1 DQS_t, DQS_c are V_{DDQ}.

NOTE 2 C2 is a don't care for 2H and 4H 3DS devices. C1 is a don't care for 2H 3DS devices.

NOTE 3 Burst Sequence driven on each DQ signal by Write Command.

Table 35 — I_{DD5B1} Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Logical Rank-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][2]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	0	**REF**	0	0	0	0	0	0	000	**0**	**0**	0	0	0	**0**	**0**	0	-
		1		1	D	1	0	0	0	0	0	000	**0**	**0**	0	0	0	**0**	**0**	0	-
				2	D	1	0	0	0	0	0	000	**0**	**0**	0	0	0	**0**	**0**	0	-
				3	D#, D#	1	1	1	1	1	0	000	**3**	**3**	0	0	0	**7**	**F**	0	-
				4	D#, D#	1	1	1	1	1	0	000	**3**	**3**	0	0	0	**7**	**F**	0	-
				4-7	repeat pattern 1...4, use **BG[1:0] = 1, BA[1:0] = 1** instead																
				8-11	repeat pattern 1...4, use **BG[1:0] = 0, BA[1:0] = 2** instead																
				12-15	repeat pattern 1...4, use **BG[1:0] = 1, BA[1:0] = 3** instead																
				16-19	repeat pattern 1...4, use **BG[1:0] = 0, BA[1:0] = 1** instead																
				20-23	repeat pattern 1...4, use **BG[1:0] = 1, BA[1:0] = 2** instead																
				24-27	repeat pattern 1...4, use **BG[1:0] = 0, BA[1:0] = 3** instead																
				28-31	repeat pattern 1...4, use **BG[1:0] = 1, BA[1:0] = 0** instead																
				32-35	repeat pattern 1...4, use **BG[1:0] = 2, BA[1:0] = 0** instead																
				36-39	repeat pattern 1...4, use **BG[1:0] = 3, BA[1:0] = 1** instead																
				40-43	repeat pattern 1...4, use **BG[1:0] = 2, BA[1:0] = 2** instead																
				44-47	repeat pattern 1...4, use **BG[1:0] = 3, BA[1:0] = 3** instead																
				48-51	repeat pattern 1...4, use **BG[1:0] = 2, BA[1:0] = 1** instead																
				52-55	repeat pattern 1...4, use **BG[1:0] = 3, BA[1:0] = 2** instead																
				56-59	repeat pattern 1...4, use **BG[1:0] = 2, BA[1:0] = 3** instead																
				60-63	repeat pattern 1...4, use **BG[1:0] = 3, BA[1:0] = 0** instead																
		2		64 ... nRFC_dlr - 1	repeat Sub-Loop 1, until nRFC_dlr - 1,Truncate, if necessary																
			1	nRFC_dlr ... 2*nRFC_dlr - 1	repeat Logical Rank-loop 0, use C[2:0]^2 = 001 instead																
			2	2*nRFC_dlr ... 3*nRFC_dlr - 1	repeat Logical Rank-loop 0, use C[2:0]^2 = 010 instead																
			3	3*nRFC_dlr ... 4*nRFC_dlr - 1	repeat Logical Rank-loop 0, use C[2:0]^2 = 011 instead																
			4	4*nRFC_dlr ... 5*nRFC_dlr - 1	repeat Logical Rank-loop 0, use C[2:0]^2 = 100 instead																
			5	5*nRFC_dlr ... 6*nRFC_dlr - 1	repeat Logical Rank-loop 0, use C[2:0]^2 = 101 instead																
			6	6*nRFC_dlr ... 7*nRFC_dlr - 1	repeat Logical Rank-loop 0, use C[2:0]^2 = 110 instead																
			7	7*nRFC_dlr ... 8*nRFC_dlr - 1	repeat Logical Rank-loop 0, use C[2:0]^2 = 111 instead																

NOTE 1 DQS_t, DQS_c are V_{DDQ}.

NOTE 2 C2 is a don't care for 2H and 4H 3DS devices. C1 is a don't care for 2H 3DS devices.

NOTE 3 DQ signals are V_{DDQ}.

Table 36 — I_{DD5B2} Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Logical Rank-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][2]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	0	**REF**	0	0	0	0	0	0	000	**0**	**0**	0	0	0	**0**	**0**	0	-
		1		1	D	1	0	0	0	0	0	000	**0**	**0**	0	0	0	**0**	**0**	0	-
				2	D	1	0	0	0	0	0	000	**0**	**0**	0	0	0	**0**	**0**	0	-
				3	D#, D#	1	1	1	1	1	0	000	**3**	**3**	0	0	0	**7**	**F**	0	-
				4	D#, D#	1	1	1	1	1	0	000	**3**	**3**	0	0	0	**7**	**F**	0	-
				4-7	repeat pattern 1...4, use **BG[1:0] = 1, BA[1:0] = 1** instead																
				8-11	repeat pattern 1...4, use **BG[1:0] = 0, BA[1:0] = 2** instead																
				12-15	repeat pattern 1...4, use **BG[1:0] = 1, BA[1:0] = 3** instead																
				16-19	repeat pattern 1...4, use **BG[1:0] = 0, BA[1:0] = 1** instead																
				20-23	repeat pattern 1...4, use **BG[1:0] = 1, BA[1:0] = 2** instead																
				24-27	repeat pattern 1...4, use **BG[1:0] = 0, BA[1:0] = 3** instead																
				28-31	repeat pattern 1...4, use **BG[1:0] = 1, BA[1:0] = 0** instead																
				32-35	repeat pattern 1...4, use **BG[1:0] = 2, BA[1:0] = 0** instead																
				36-39	repeat pattern 1...4, use **BG[1:0] = 3, BA[1:0] = 1** instead																
				40-43	repeat pattern 1...4, use **BG[1:0] = 2, BA[1:0] = 2** instead																
				44-47	repeat pattern 1...4, use **BG[1:0] = 3, BA[1:0] = 3** instead																
				48-51	repeat pattern 1...4, use **BG[1:0] = 2, BA[1:0] = 1** instead																
				52-55	repeat pattern 1...4, use **BG[1:0] = 3, BA[1:0] = 2** instead																
				56-59	repeat pattern 1...4, use **BG[1:0] = 2, BA[1:0] = 3** instead																
				60-63	repeat pattern 1...4, use **BG[1:0] = 3, BA[1:0] = 0** instead																
		2		64 ... nRFC_slr - 1	repeat Sub-Loop 1, until nRFC_slr - 1,Truncate, if necessary																
			1	nRFC_slr ... 2*nRFC_slr - 1	repeat Logical Rank-loop 0																
			2	2*nRFC_slr ... 3*nRFC_slr - 1	repeat Logical Rank-loop 0																
			3	3*nRFC_slr ... 4*nRFC_slr - 1	repeat Logical Rank-loop 0																
			4	4*nRFC_slr ... 5*nRFC_slr - 1	repeat Logical Rank-loop 0																
			5	5*nRFC_slr ... 6*nRFC_slr - 1	repeat Logical Rank-loop 0																
			6	6*nRFC_slr ... 7*nRFC_slr - 1	repeat Logical Rank-loop 0																
			7	7*nRFC_slr ... 8*nRFC_slr - 1	repeat Logical Rank-loop 0																

NOTE 1 DQS_t, DQS_c are V_{DDQ}.

NOTE 2 C2 is a don't care for 2H and 4H 3DS devices. C1 is a don't care for 2H 3DS devices.

NOTE 3 DQ signals are V_{DDQ}.

Table 37 — I_{DD7} Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][2]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
toggling	Static High	0	0	**ACT**	0	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	**-**
			1	**RDA**	0	1	1	0	1	0		**0**	**0**	0	0	1	**0**	**0**	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			2	D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			3	D#	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
			...	repeat pattern 2...3 until nRRD - 1, if nRCD > 4. Truncate if necessary																
		1	nRRD	**ACT**	0	0	0	0	0	0	0	**1**	**1**	0	0	0	**0**	**0**	0	**-**
			nRRD + 1	**RDA**	0	1	1	0	1	0		**1**	**1**	0	0	1	**0**	**0**	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			...	repeat pattern 2 ... 3 until 2*nRRD - 1, if nRCD > 4. Truncate if necessary																
		2	2*nRRD	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 2** instead																
		3	3*nRRD	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 3** instead																
		4	4*nRRD	repeat pattern 2 ... 3 until nFAW - 1, if nFAW > 4*nRCD. Truncate if necessary																
		5	nFAW	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 1** instead																
		6	nFAW + nRRD	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 2** instead																
		7	nFAW + 2*nRRD	repeat Sub-Loop 0, use **BG[1:0] = 0, BA[1:0] = 3** instead																
		8	nFAW + 3*nRRD	repeat Sub-Loop 1, use **BG[1:0] = 1, BA[1:0] = 0** instead																
		9	nFAW + 4*nRRD	repeat Sub-Loop 4																
		10	2*nFAW	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 0** instead																
		11	2*nFAW + nRRD	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 1** instead																
		12	2*nFAW + 2*nRRD	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 2** instead																
		13	2*nFAW + 3*nRRD	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 3** instead																
		14	2*nFAW + 4*nRRD	repeat Sub-Loop 4																
		15	3*nFAW	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 1** instead																
		16	3*nFAW + nRRD	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 2** instead																
		17	3*nFAW + 2*nRRD	repeat Sub-Loop 0, use **BG[1:0] = 2, BA[1:0] = 3** instead																
		18	3*nFAW + 3*nRRD	repeat Sub-Loop 1, use **BG[1:0] = 3, BA[1:0] = 0** instead																
		19	3*nFAW + 4*nRRD	repeat Sub-Loop 4																
		20	4*nFAW	repeat pattern 2 ... 3 until nRC - 1, if nRC > 4*nFAW. Truncate if necessary																

NOTE 1 DQS_t, DQS_c are V_{DDQ}.
NOTE 2 C2 is a don't care for 2H and 4H 3DS devices. C1 is a don't care for 2H 3DS devices.
NOTE 3 Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are V_{DDQ}.

10.2 I_{DD} and I_{PP} Specifications

I_{DD} and I_{PP} values are for full operating range of voltage and temperature unless otherwise noted.

Table 38 — I_{DD} and I_{DDQ} Specification Example

Speed Grade Bin				NOTE
Symbol		I_{PP} Max.		
I_{DD0}			mA	
I_{DD0A}			mA	
I_{DD1}			mA	
I_{DD1A}			mA	
I_{DD2N}			mA	
I_{DD2NA}			mA	
I_{DD2NT}			mA	
I_{DDQ2NT}			mA	
I_{DD2P}			mA	
I_{DD2Q}			mA	
I_{DD3N}			mA	
I_{DD3NA}			mA	
I_{DD3P}			mA	
I_{DD4R}			mA	
I_{DD4RA}			mA	
I_{DDQ4R}			mA	
I_{DD4W}			mA	
I_{DD4WA}			mA	
I_{DD4WC}			mA	
I_{DD4W_par}			mA	
I_{DD5B1}			mA	
I_{DD5B2}			mA	
I_{DD6}			mA	
I_{DD6E}[1]			mA	
I_{DD6N}			mA	
I_{DD6R}			mA	
I_{DD6A}			mA	
I_{DD7}			mA	
I_{DD8}			mA	
NOTE 1 Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR4 3D Stacked SDRAM devices support the following options or requirements referred to in this material.				

10.2 I_{DD} and I_{PP} Specifications (cont'd)

Table 39 — I_{PP} and I_{PPQ} Specification Example

Speed Grade Bin				NOTE
Symbol		I_{PP} Max.		
I_{PP0}			mA	
I_{PP1}			mA	
I_{PP2N}			mA	
I_{PP2P}			mA	
I_{PP3N}			mA	
I_{PP3P}			mA	
I_{PP4R}			mA	
I_{PP4W}			mA	
I_{PP5B}			mA	
I_{PP5F2}			mA	
I_{PP5F4}			mA	
I_{PP6E}[1]			mA	
I_{PP6N}			mA	
I_{PP6R}			mA	
I_{PP6A}			mA	
I_{PP7}			mA	
I_{PP8}			mA	
NOTE 1 Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR4 3D Stacked SDRAM devices support the following options or requirements referred to in this material.				

10.2 I_{DD} and I_{PP} Specifications (cont'd)

Table 40 — I_{DD6} Specification

Symbol	Temperature Range		Unit	Notes
I_{DD6N}	0 - 85 °C		mA	2, 3
I_{DD6E}	0 - 95 °C		mA	3, 4, 5
I_{DD6R}	0 - 45 °C		mA	3, 4, 8
I_{DD6A}	0 °C ~ T_a		mA	3, 5, 6, 7
	T_b ~ T_y		mA	3, 5, 6, 7
	T_z ~ $T_{OPERmax}$		mA	3, 5, 6, 7

NOTE 1 Max. values for I_{DD} currents considering worst case conditions of process, temperature and voltage.

NOTE 2 Applicable for MR2 settings A6=0 and A7=0.

NOTE 3 Supplier data sheets include a max value for I_{DD6}.

NOTE 4 Applicable for MR2 settings A6=0 and A7=1. I_{DD6E} is only specified for devices which support the Extended Temperature Range feature.

NOTE 5 Refer to the supplier data sheet for the value specification method (e.g., max, typical) for I_{DD6E} and I_{DD6A}

NOTE 6 Applicable for MR2 settings A6=1 and A7=0. I_{DD6A} is only specified for devices which support the Auto Self Refresh feature.

NOTE 7 The number of discrete temperature ranges supported and the associated T_a - T_z values are supplier/ design specific. Temperature ranges are specified for all supported values of T_{OPER}. Refer to supplier data sheet for more information.

NOTE 8 Applicable for MR2 settings TBD. I_{DD6R} is verified by design and characteriation, and may not be subject to production test.

11 Input/Output Capacitance

Table 41 — DDR4 3DS Silicon pad I/O Capacitance

Symbol	Parameter	DDR4-1600,1866, 2133		DDR4-2400,2666		DDR4-3200		Unit	NOTE
		min	max	min	max	min	max		
C_{IO}	Input/output capacitance	0.7	1.6	0.7	1.5	TBD	TBD	pF	1,2,3
C_{DIO}	Input/output capacitance delta	-0.1	0.1	-0.1	0.1	TBD	TBD	pF	1,2,3,11
C_{DDQS}	Input/output capacitance delta DQS_t and DQS_c		0.05		0.05	TBD	TBD	pF	1,2,3,5
C_{CK}	Input capacitance, CK_t and CK_c	0.2	0.8	0.2	0.7	TBD	TBD	pF	1,3
C_{DCK}	Input capacitance delta CK_t and CK_c		0.05		0.05	TBD	TBD	pF	1,3,4
C_I	Input capacitance(CTRL, ADD, CMD pins only)	0.2	0.8	0.2	0.7	TBD	TBD	pF	1,3,6
C_{DI_CTRL}	Input capacitance delta(All CTRL pins only)	-0.1	0.1	-0.1	0.1	TBD	TBD	pF	1,3,7,8
$C_{DI\_ADD\_CMD}$	Input capacitance delta(All ADD/ CMD pins only)	-0.1	0.1	-0.1	0.1	TBD	TBD	pF	1,2,9,10
C_{ALERT}	Input/output capacitance of ALERT	0.5	2.5	0.5	2.5	TBD	TBD	pF	1,3
C_{ZQ}	Input/output capacitance of ZQ	0.5	2.5	0.5	2.5	TBD	TBD	pF	1,3,12

NOTE 1 This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ} applied with all other signal pins floating. Measurement procedure tbd.

NOTE 2 DQ, DM_n, DQS_T, DQS_C, TDQS_T, TDQS_C. Although the TDQS_T and TDQS_C pins have different functions, the loading matches DQ and DQS

NOTE 3 This parameter applies to 3DS devices. It is meant to represent the silicon pad capacity of the master die.

NOTE 4 Absolute value CK_T-CK_C

NOTE 5 Absolute value of CIO(DQS_T)-CIO(DQS_C)

NOTE 6 CI applies to ODT, CS_n, CKE, A0-A17, BA0-BA1, BG0-BG1, RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.

NOTE 7 CDI CTRL applies to ODT, CS_n and CKE

NOTE 8 CDI_CTRL = CI(CTRL)-0.5*(CI(CLK_T)+CI(CLK_C))

NOTE 9 CDI_ADD_ CMD applies to, A0-A17, BA0-BA1, BG0-BG1,RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.

NOTE 10 CDI_ADD_CMD = CI(ADD_CMD)-0.5*(CI(CLK_T)+CI(CLK_C))

NOTE 11 CDIO = CIO(DQ,DM)-0.5*(CIO(DQS_T)+CIO(DQS_C))

NOTE 12 Maximum external load capacitance on ZQ pin: tbd pF.

The DDR4 3DS package electrical specifications are TBD and may NOT be the same as for the mono SDRAM in JESD79-4.

12 Electrical Characteristics and AC Timings for DDR4-1600-3DS to DDR4-2400-3DS

12.1 Refresh parameters

Typical platforms are designed with the assumption that no more than one physical rank is refreshed at the same time. In order to limit the maximum refresh current (I_{DD5B1}) for a 3D stacked SDRAM, it will be required to stagger the refreshes to each device in a stack.

The tRFC time for a single logical rank is defined as tRFC_slr and is specified as the same value as for a monolithic DDR4 SDRAM of equivalent density. The minimum amount of stagger between refresh commands (=tREF_stagger) sent to different logical ranks is specified to be approximately tRFC_slr/3 - Table 42.

Table 42 — Refresh parameters by logical rank density

Parameter	Symbol		Logical Rank Density			Units	Note
			4 Gb	8 Gb	16 Gb		
REF command to ACT or REF command time to same logical rank	tRFC_slr1 (1X mode)		260	350	TBD1	ns	
	tRFC_slr2 (2X mode)		160	260	TBD2	ns	
	tRFC_slr4 (4X mode)		110	160	TBD3	ns	
REF command to REF command to different logical rank	tRFC_dlr1 (1X mode)		90	120	TBD1/3	ns	
	tRFC_dlr2 (2X mode)		55	90	TBD2/3	ns	
	tRFC_dlr4 (4X mode)		40	55	TBD3/3	ns	
Average periodic refresh interval in same logical rank	tREFI_slr1 (1X mode)	0 °C =< T_{CASE} =< 85 °C	7.8	7.8	TBD4	us	
		85 °C < T_{CASE} =< 95 °C	3.9	3.9	TBD4/2	us	
	tREFI_slr2 (2X mode)	0 °C =< T_{CASE} =< 85 °C	3.9	3.9	TBD4/2	us	
		85 °C < T_{CASE} =< 95 °C	1.95	1.95	TBD4/4	us	
	tREFI_slr4 (4X mode)	0 °C =< T_{CASE} =< 85 °C	1.95	1.95	TBD4/4	us	
		85 °C < T_{CASE} =< 95 °C	0.975	0.975	TBD4/8	us	

12.2 Timing Parameters by Speed Grade

Table 43 — Timing Parameters by Speed Bin for DDR4-1600-3DS to DDR4-1866-3DS

Parameter	Symbol	DDR4-1600-3DS		DDR4-1866-3DS		Units	Note
		Min	Max	Min	Max		
Row Activate to Row Activate Delay							
ACTIVATE to ACTIVATE command period to different bank group in the same logical rank	tRRD_S_slr	max(4nCK, 5ns)	-	max(4nCK, 4.2ns)	-	ns	
ACTIVATE to ACTIVATE command period to same bank group in the same logical rank	tRRD_L_slr	max(4nCK, 6ns)	-	max(4nCK, 5.3ns)	-	ns	
ACTIVATE to ACTIVATE command period to different logical ranks	tRRD_dlr	4	-	4	-	nCK	
Four Activate Window							
Four activate window to the same logical rank for 0.5 KB page size	tFAW_slr_x4	20	-	17	-	ns	1
Four activate window to the same logical rank for 1 KB page size	tFAW_slr_x8	25	-	23	-	ns	2
Four activate window to different logical ranks	tFAW_dlr	16	-	16	-	nCK	
Self-Refresh Timings							
Exit Self-Refresh to commands not requiring a locked DLL	tXS	max(5nCK, tRFC_slr(min) + 10ns)		max(5nCK, tRFC_slr(min) + 10ns)			3

NOTE 1 For x4 devices only.

NOTE 2 For x8 devices only.

NOTE 3 Upon exit from Self-Refresh, the 3D Stacked DDR4 SDRAM requires a minimum of one extra refresh command to all logical ranks before it is put back into Self-Refresh Mode.

12.2 Timing Parameters by Speed Grade (cont'd)

Table 44 — Timing Parameters by Speed Bin for DDR4-2133-3DS to DDR4-2400-3DS

Parameter	Symbol	DDR4-2133-3DS		DDR4-2400-3DS		Units	Note
		Min	Max	Min	Max		
Row Activate to Row Activate Delay							
ACTIVATE to ACTIVATE command period to different bank group in the same logical rank	tRRD_S_slr	max(4nCK, 3.7ns)	-	max(4nCK, 3.3ns)	-	ns	
ACTIVATE to ACTIVATE command period to same bank group in the same logical rank	tRRD_L_slr	max(4nCK, 5.3ns)	-	max(4nCK, 4.9ns)	-	ns	
ACTIVATE to ACTIVATE command period to different logical ranks	tRRD_dlr	4	-	4	-	nCK	
Four Activate Window							
Four activate window to the same logical rank for 0.5KB page size	tFAW_slr_x4	15		13	-	ns	1
Four activate window to the same logical rank for 1KB page size	tFAW_slr_x8	21		21	-	ns	2
Four activate window to different logical ranks	tFAW_dlr	16	-	16	-	nCK	
Self-Refresh Timings							
Exit Self-Refresh to commands not requiring a locked DLL	tXS	max(5nCK, tRFC_slr(min) + 10ns)		max(5nCK, t_{RFC}_slr(min) + 10ns)			3

NOTE 1 For x4 devices only.

NOTE 2 For x8 devices only.

NOTE 3 Upon exit from Self-Refresh, the 3D Stacked DDR4 SDRAM requires a minimum of one extra refresh command to all logical ranks before it is put back into Self-Refresh Mode.

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